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A New 7-Level Inverter for Active and Reactive Power Compensation Using PEV in Grid-Connected Applications

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Abstract – Typically, conventional multilevel inverters (MLI) have the disadvantage of being unable to step up the input voltage. Therefore, one type of three phase MLI with boost capacity is proposed. The proposed three-phase inverter is capable of generating seven levels (0, 1Vdc, 2Vdc, 3Vdc, -1Vdc, -2Vdc, -3Vdc), while only one DC source and five capacitors are required for the three phase configuration. To facilitate analysis, a phase position pulse-width-modulation (PD-PWM) strategy is applied to control switches. And suitable switching modes are also selected to balance the voltage of capacitors. In order to verify and validate the proper operation of the proposed circuit configuration and the ability using plug-in electric vehicle (PVE) battery into grid, the system is simulated in PLECS. The results of simulation are provided to validate the feasibility of the proposed inverter.

Keywords – Multilevel inverter, PVE, Vehicle-to-grid (V2G) application, Switched capacitor, PD-PWM.

I. INTRODUCTION

Multilevel inverter has been intensively studied in the literature for diverse range of applications, such as renewable energy conversion systems, high-voltage DC applications, and distributed generation systems. The application of V2G is one of the prospering new energy, which provide bi-directional power transmission between PVE batteries and the grid, and provide ancillary services to the grid. V2G can be applied in voltage regulation, frequency regulation and rotating reserve of the grid. In order to realized the application of V2G, the study of grid-connected inverters as well as control makes it possible [1]. Due to MLI's remarkable advantages such as near-sinusoidal output voltage waveform; low EMI, higher voltage power conversion [2]-[5]. There are three type of Conventional MLI topologies: the neutral-point-clamped (NPC) MLI, flying capacitor (FC) MLI and cascaded H-bridge (CHB) MLI [6]-[10]. These topologies have become remarkably mature in certain applications. For example, CHB MLI is extensively employed in photovoltaic (PV) systems, electric vehicles(EV), etc., which needs more H-bridge units to be cascaded for handling the higher power, resulting higher system costs [6]. On the other hand, FC MLI and NPC MLI are also well used in PV or EV system, driver applications. As the output level increasing, problems with voltage balance and failure rate of inverter are inevitable owing to the large number of components connected in the conventional inverter structures [7], [10].

Therefore, many researchers have made improvements based on conventional MLIs to obtain more competitive MLIs. Switched capacitor MLIs technology have the advantage of its flexible structure [10]. Hence, linking the switched capacitor structure with the conventional MLI structure became popular among researchers. in [12], a new type of active neutral clamp (ANPC) inverter can generate 7-levels is proposed. Additional voltage balancing circuits is required for this topology to balance the DC link capacitor's voltage, making the system more complicated. A hybrid 7-level ANPC topology is presented in [13], which used harmonic elimination to obtain an output voltage with lower harmonic distortion. However, the value of output voltage is smaller than the value of DC source, which means it has no boost capability. A 7-level inverter based on a T-type topology is introduced in [14] by using a floating capacitor unit to increase the number of output levels, but the output voltage is still half of the input voltage. As described above, the disadvantage the topology [12]-[14] is that additional circuit is required to regulate the floating capacitor's voltage.

To overcome these drawbacks mentioned above, resent topologies are proposed utilizing capacitor voltage self-balancing techniques to improve conventional MLI topologies. Two ANPC topologies with capacitor' voltage self-balancing capability and boosting capability have been presented in [15] and [16]. However, these topologies are still demanding a large number of switching elements and have a high DC link voltage.

With the aim of achieving a high gain, capacitor voltage self-balance and low-voltage stress, a new 7-level inverter based on a conventional T-type inverter is proposed. The proposed topology has a boost capacity of 1.5 times to the value of input voltage and more effectively utilizing the voltage of DC-link capacitors than conventional MLIs topology. Meanwhile, the proposed inverter fed by PVE's battery for compensating active and reactive power of the grid is verified using a power direct control strategy. The proposed topology is depicted in Fig.1, and simultaneous structural diagram of the grid-connected control block diagram is show in Fig.2.

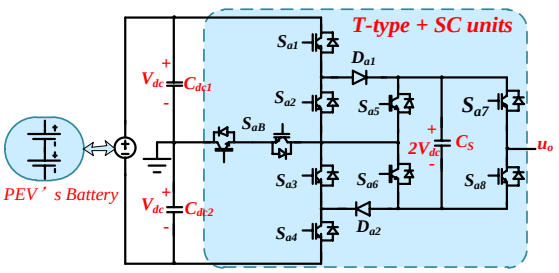


Fig.1: Proposed single phase of 7-level inverter

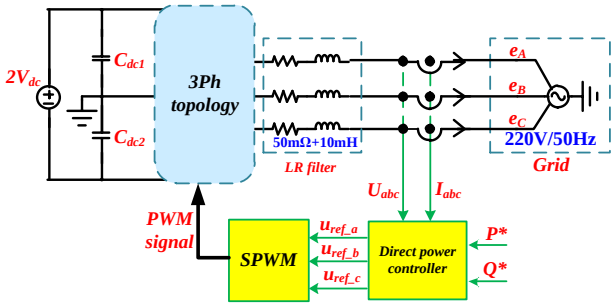


Fig.2: The schematic of direct power control strategy

II. Circuit Descriptions and Operating Principles

In order to facilitate the analysis, phase A is taken as an example for the following analysis. The phase A topology of the proposed seven-level boost inverter is depicted in Fig.1. the value of input voltage is $2V_{dc}$, u_o is equal to the output voltage, Cs is switched capacitor, C_{dc1} and C_{dc2} are the DC-Link capacitors. C_{dc1} has the same value as C_{dc2}, meaning that they have a uniform input voltage distribution. The switched capacitor is connected in parallel to the input voltage source through diodes D_{a1} and D_{a2}, which charge the voltage to the $+2V_{dc}$ at output voltage $\pm 1V_{dc}$. With the operation of switches S_{a1}-S_{a8} and S_{aB}, the proposed inverter is capable of generating seven-level voltage, and the maximum output voltage up to $+3V_{dc}$, thus achieving the boost capacity of 1.5 times. The states of switches and Cs for each output voltage are illustrated in Tab I.

As illustrated in Table I, this inverter is able to generate seven levels of 0, $\pm 1V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$. The state analysis of the positive half cycle (Mode 1-4) is shown in Fig.3.

Mode 4, the output level of the inverter is 0 as shown in Fig.3(a), the output terminal of the inverter is connected to the neutral ground through bidirectional switches S_{aB}, S_{a2}, D_{a1} and S_{a7}, and the other switching states as illustrated in Table I. The state of switched capacitor is idle.

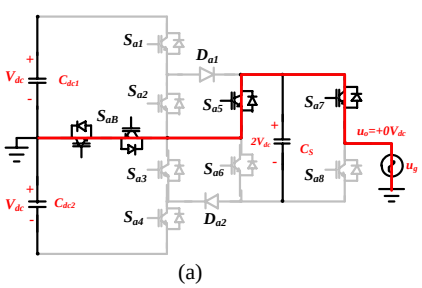
Mode 3, the output level of the inverter is $+1V_{dc}$ as shown in Fig.3(b), the output terminal of the inverter is connected to C_{dc1}'s positive terminal through the switches S_{a1}, D_{a1} and S_{a7} , and the other switching states as illustrated in Table I. The switched capacitor is connected in parallel with the input power supply. And its voltage is charged to $2V_{dc}$.

Mode 2, the inverter's output level is equal to $+2V_{dc}$ as illustrated in Fig.3(c), the inverter utilizes switched capacitor to provide energy output for the load through the bidirectional switch S_{aB}, S_{a6} and S_{a7}, which results in the switched capacitor's voltage drop. The other switching states is illustrated in Table I.

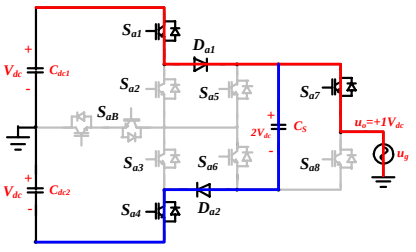
Mode 1, the inverter's output level is equal to $+3V_{dc}$ as illustrated in Fig.3(d), the switched capacitor is directly connected to C_{dc1} to provide energy output for the load through the bidirectional switch S_{aB}, S_{a1}, S_{a2}, S_{a6} and S_{a7}, which results the switched capacitor's voltage drop. The other switching states is illustrated in Table I.

Table 1: The working states for the phase A

Mode	Cs	Switching states			Output levels
		S_{aB}	S_{a1}~S_{a4}	S_{a5}~S_{a8}	
1	Discharge	0	1100	1010	$+3V_{dc}$
2	Discharge	1	0000	1010	$+2V_{dc}$
3	Charge	0	1001	0010	$+1V_{dc}$
4	Idle	1	0000	1010	$+0V_{dc}$
5	Idle	1	0000	0101	$-0V_{dc}$
6	Charge	0	1001	0001	$-1V_{dc}$
7	Discharge	1	0000	0101	$-2V_{dc}$
8	Discharge	0	0011	0101	$-3\ V_{dc}$



(a)



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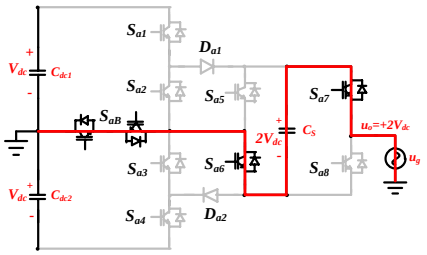
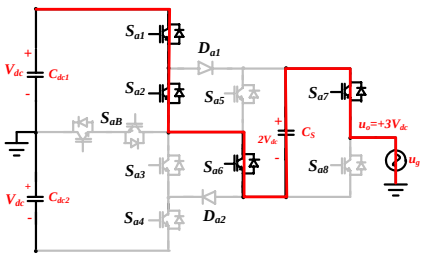


(c)



(d)

Fig.3: Operation modes of the proposed inverter: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4 .

III. Modulation and Capacitor Voltage Ripple

A. Modulation

In order to improve the quality of energy produced by MLIs, the fundamental frequency modulation or high frequency modulation can be used to make the inverter output sinusoidal voltage[10]. For the purpose of facilitating analysis, PD-PWM strategy is employed for the proposed multilevel circuits.

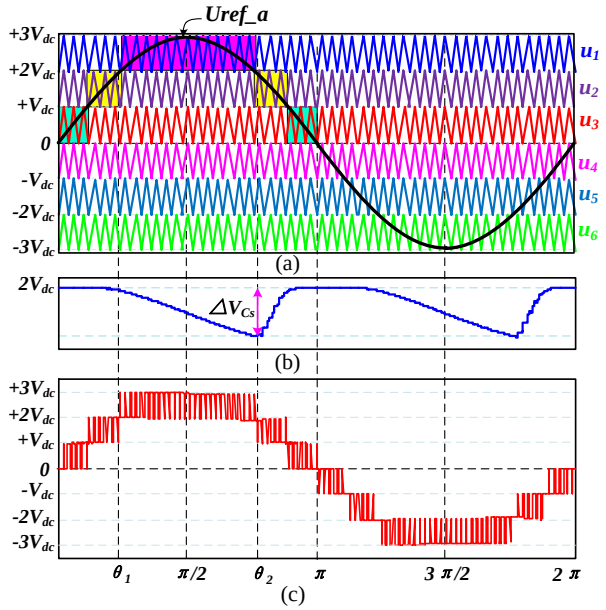


Fig. 4: The scheme of adopted PD-PWM.

Assume that the modulation waveform expression of phase A is :

$$u_{ref\_a} = 3V_{dc} \cdot m \cdot \sin(\omega t) \quad (1)$$

where m is the modulation index, $m \in (0,1)$.

As depicted in Fig.4(a), the PWM pulse of the switches is obtained by comparing the modulation signal(u_{ref_a}) with the carrier signals (u_1-u_6).

In Sector 1, reference waveform u_{ref_a} is compared with the carrier signal u_3 to generate an output level of 0 to $+1V_{dc}$.

In Sector 2, the modulation signal u_{ref_a} is compared with the carrier signal u_2 to generate an output voltage of $+1V_{dc}$ to $+2V_{dc}$.

In Sector 3, reference waveform u_{ref_a} is compared to the triangle signal u_1 to generate an output voltage from $+2V_{dc}$ to $+3V_{dc}$. Due to the symmetry of the modulation waveform, the principle of negative half cycle is the same as what was previously described. Eventually, the waveform of the output voltage waveform in phase A is shown in Fig.4(c).

B. Design Guideline of Capacitor

For the purpose of reducing the voltage ripple of *Cs* to enhance the power quality, it is essential to keep the voltage of *Cs* fluctuating within a certain range. During an output voltage of $\pm 3V_{dc}$, the capacitor *Cs* continuously provides energy to the load. When inverter output voltage is equal to $u_O = \pm 1V_{dc}$, *Cs* is in the state of charging and discharging alternately. When the output voltage is $0V_{dc}$,the *Cs* is connected in parallel with DC source. And *Cs* is in the state of idle. As is illustrated in Table 1.

As is shown in Fig.3(c), (d), the discharge current of *Cs* is the load current i_O, therefore, the amount of discharge of the capacitor *Cs* can be simply described as

$$\Delta Q = \frac{1}{C_s}\int_{t_1}^{t_2} i_O \, dt \quad (2)$$

where t_1 to t_2 is the duration of capacitor discharging time.

As shown in Fig. 4(b), for one cycle of the output voltage, the capacitor *Cs* has two continuous discharging periods i.e. $u_O = +2V_{dc}$. As a result, the amount of discharge ΔQ of C_S can be estimated by

$$\Delta Q = \frac{1}{2\pi f C_s}\int_{\theta_1}^{\theta_2} i_o d\omega t \quad (3)$$

where θ_1 and θ_2 are the conducting angle corresponding to $u_O = +2V_{dc}$, as depicted in Fig. 4(c); f is the frequency of the output voltage of proposed three-phase inverter .

Substituting $\theta_1 = \arcsin(2/3m)$ and $\theta_2 = \pi - \theta_1$ into (3), the expression can be derived as

$$\Delta Q = \frac{2V_{dc}}{2\pi f R C_s}\sqrt{9m^2 - 4} \quad (4)$$

It means that the amount of discharge is negatively correlated with frequency and load.

It can be further obtained from (4), the value of the capacitor *Cs* can be determined from the following equation within the allowable voltage ripple rating δ :

$$C_s = \frac{1}{\delta \pi f R}\sqrt{\left(\frac{3m}{2}\right)^2 - 1} \quad (5)$$

IV. Direct Power Control

To make the proposed inverter operate smoothly connected to the grid, a dual closed-loop controller is used to control the active and reactive power of proposed inverter in grid-connected application.

Assuming that the equivalent resistance of each phase on the output side of the grid-connected inverter and the grid-connected equivalent inductance are *R*, *L*,

respectively, the following relationship can be obtained from Fig.2 and the Kirchhoff voltage equation:

$$\begin{cases} u_A = Ri_A + L\dfrac{di_A}{dt} + e_A \\ u_B = Ri_B + L\dfrac{di_B}{dt} + e_B \\ u_C = Ri_C + L\dfrac{di_C}{dt} + e_C \end{cases} \quad (6)$$

where e_A , e_B, e_C are output voltage of grid.

The equation of the grid voltage in the d, q coordinate system can be obtained using the Park transform with rotation d, q coordinate system:

$$\begin{cases} u_d = Ri_d + L\dfrac{di_d}{dt} + e_d - L\omega i_q \\ u_q = Ri_q + L\dfrac{di_q}{dt} + e_q + L\omega i_d \end{cases} \quad (7)$$

In order to achieve complete decoupling of active and reactive power, and the PI controller is used to adjust the active and reactive currents. It is assumed that:

$$\begin{cases} \Delta u_d = Ri_d + L\dfrac{di_d}{dt} = PI(i_d{}^*, i_d) \\ \Delta u_q = Ri_q + L\dfrac{di_q}{dt} = PI(i_q{}^*, i_q) \end{cases} \quad (8)$$

Substitute equation (8) into equation (7), and the following equation is obtained:

$$\begin{cases} u_d{}^* = \Delta u_d - L\omega i_q + e_d \\ u_q{}^* = \Delta u_q + L\omega i_d + e_q \end{cases} \quad (9)$$

From the analysis above, the specific control strategy of the power external loop control of the grid-connected inverter can be obtained, as shown in Fig. 5.

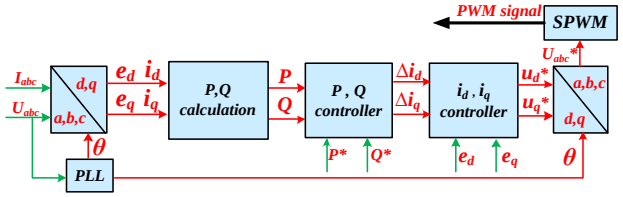


Fig. 5: The control strategy for grid-connected inverter

V. Simulation Results

To verify the feasibility of the proposed MLI and the stable operation of grid-connected control, a simulated model was created in PLECS referring Fig. 2. The system parameters are listed in Table2.

Condition 1: The voltage of 300V DC source is used in the simulation. the P* is equal to 1KW in 0 to 0.2s, 3KW in 0.2-0.5s, and 6KW in 0.5-1s. In order to make the proposed inverter operate in the unit power factor state with, i. e. the reactive power is equal to 0. The simulation results are presented in Figure 6(a), (b) and (c).

Table 2: Simulation of the system parameters

Parameter	Value
DC source $2V_{dc}$	***300V***
DC bus capacitors C_{dc}	***4000uF***
Capacitor Cs	***2000uF***
Filter R, L	***0.5ohm,10mH***
Grid phase voltage(RMS) e	***220V***
Grid frequency f	***50Hz***

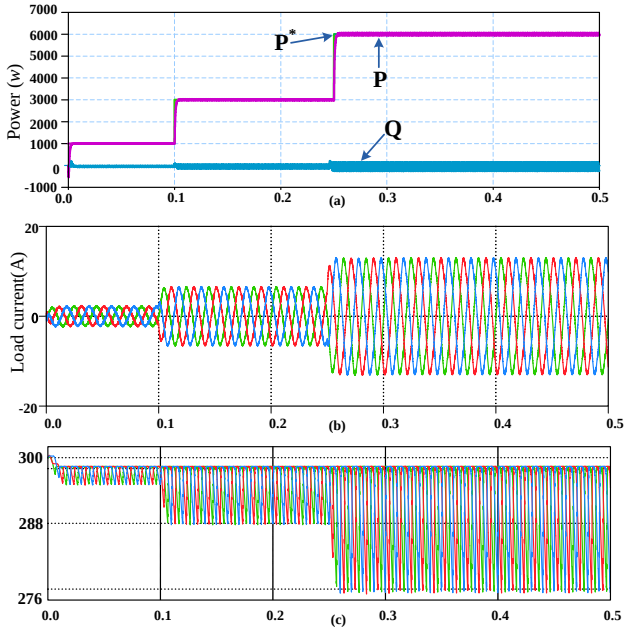


Fig. 6: The result of simulation: (a) *P*,*Q* under condition 1, (b) Load current waveform, (c) Voltage waveform of *Cs*

The results of the control of active P and active power Q are shown in Fig.6(a), and the waveform of three-phase grid current is shown in Fig.6(b). it can be clearly seen from Fig.6(a) that the active power output from the inverter is able to smoothly track the reference power when a given active power is suddenly change. Meanwhile, the load current can be quickly adjusted in response to changing output power of the inverter. The voltage ripple waveform of switched capacitor *Cs* is depicted in Fig.6(c). As proposed inverter's output power become large, the output current becomes larger which leads to larger ripple of the capacitor *Cs* at 0.1s and 0.25s, which verifies the section III.

Condition 2: The voltage of 300V DC source is used in the simulation. The active power is equal to 2KW from 0 to 0.2s, and then stepped up to 6KW at 0.2s. The reactive Q* is 0VAR at 0-0.3s, and then stepped up to 2000VAR at 0.3s. The other parameters are maintained identical. The simulation results are presented in Fig.7 (a), (b) and (c).

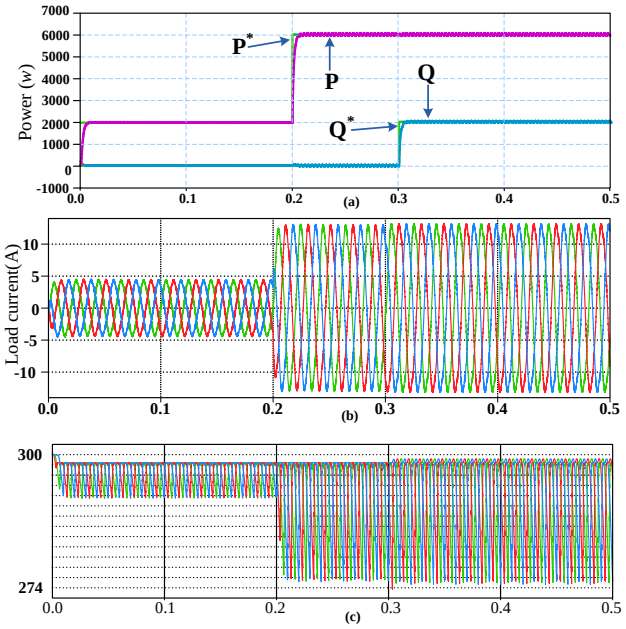


Fig. 7: The result of simulation: (a) *P*,*Q* under condition 2, (b) Load current waveform, (c) Voltage waveform of *Cs*

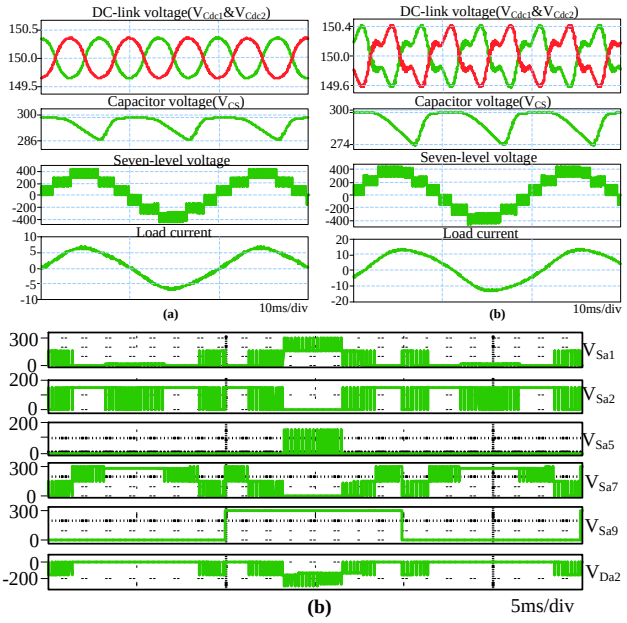


Fig. 8: Main waveforms of the proposed seven-level inverter : (a) Output voltage and current waveforms under condition 1, (b) Output voltage and current waveforms under condition 2, (c) Voltage waveform of witches and diode

The control results for active and active power are presented in Fig.7(a). The output current waveform of inverter is shown in Fig.7(b). The result that shown in Fig.7(a), (b) that the power provided by the proposed inverter can smoothly track the changes of a given power as the active power suddenly steps from 2KW to 6KW at 0.2s. Meanwhile, the inverter current can also be adjusted quickly. The ripple voltage of switched capacitor are shown in Fig.7(c), which indicates that the voltage ripple of the capacitor remains stable after a sudden change in the given reactive power, due to the inverter output current amplitude remaining constant.

Fig.8 shows the steady-state output voltage, the grid-connected current, and the voltage of the *Cs* and DC-link capacitor in the condition 1 (P=3000W). in the case that the power factor is equal to 1, the current and voltage are in phase. The voltage across the switched capacitor *Cs* and DC-link capacitor can be naturally balanced around its reference value, as shown is Fig.6(c) and Fig.8(a). Meanwhile, the inverter is also able to provide a stable output 7-level voltage. And the output voltage is 1.5 times the input DC voltage. When the system adds reactive power regulation, the voltages of the *Cs* and DC-link capacitor are also automatically balanced, as shown in Fig.7(c) and Fig.8(b). The devices voltage stress of the proposed topology, it can be seen that the voltage stress of topology's devices are less than or equal to input voltage.

V. Conclusion

In this paper, a type of three phase multilevel inverter with boost capacity is proposed for grid-connected application. The proposed inverter is introduced based on switched capacitor and T-type circuit structure. The switched capacitor is designed by theoretically analyzing so that the capacitor's voltage ripple stays within allowable limit. The power direct control strategy is also analyzed and designed to achieve the compensation of active and reactive power of the grid using PVE battery. The theoretical analysis is validated through simulation.

References

[1] W. Choi, W. Lee and B. Sarlioglu, "Reactive power compensation of grid-connected inverter in vehicle-to-grid application to mitigate balanced grid voltage sag," 2016 IEEE Power and Energy Society General Meeting (PESGM), Boston, MA, 2016

[2] N. A. Rahim, K. Chaniago and J. Selvaraj, "Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System," in IEEE Transactions on Industrial Electronics, vol. 58, no. 6, pp. 2435-2443, June 2011.

[3] A. Riyaz, A. Iqbal and M. Tariq, "Five-Phase Twenty-Seven Level Inverter Using Single DC Source for Photovoltaic Application," 2020 IEEE International Conference on Computing, Power and Communication Technologies (GUCON), Greater Noida, India, 2020.

[4] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, "The age of multilevel converters arrives," in IEEE Industrial Electronics Magazine, vol. 2, no. 2, pp. 28-39, June 2008.

[5] W. Peng, Y. Ye and B. Jiang, "Cost-effective solution of EV motor driver based on asymmetric cascaded multilevel inverters," 2017 7th International Conference on Power Electronics Systems and Applications - Smart Mobility, Power Transfer & Security (PESA), Hong Kong, 2017

[6] J. C. Kartick, B. K. Sujit and K. Suparna, "Dual reference phase shifted pulse width modulation technique for a N-level inverter based grid connected solar photovoltaic system," in IET Renewable Power Generation, vol. 10, no. 7, pp. 928-935, 7 2016.

[7] A. Edpuganti and A. K. Rathore, "Fundamental Switching Frequency Optimal Pulsewidth Modulation of Medium-Voltage Nine-Level Inverter," in IEEE Transactions on Industrial Electronics, vol. 62, no. 7, pp. 4096-4104, July 2015.

[8] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A survey on neutral-point-clamped inverters", IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219-2230, Jul. 2010..

[9] M. Malinowski, K. Gopakumar, J. Rodriguez and M. Perez, "A survey on cascaded multilevel inverters", IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197-2206, Jul. 2010.

[10] A. Ghias, J. Pou, V. Agelidis and M. Ciobotaru, "Initial capacitor charging in grid-connected flying capacitor multilevel converters", IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3245-3249, Jul. 2014.

[11] Y. Ye, K. W. E. Cheng, J. Liu and K. Ding, "A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing," in IEEE Transactions on Industrial Electronics, vol. 61, no. 12, pp. 6672-6680, Dec. 2014,

[12] M. Saeedifard, P. M. Barbosa and P. K. Steimer, "Operation and Control of a Hybrid Seven-Level Converter," in IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 652-660, Feb. 2012

[13] S. R. Pulikanti, G. Konstantinou and V. G. Agelidis, "Hybrid Seven-Level Cascaded Active Neutral-Point-Clamped-Based Multilevel Converter Under SHE-PWM," in IEEE Transactions on Industrial Electronics, vol. 60, no. 11, pp. 4794-4804, Nov. 2013

[14] H. Vahedi and K. Al-Haddad, "Real-Time Implementation of a SevenLevel Packed U-Cell Inverter with a Low-Switching-Frequency Voltage Regulator," IEEE Trans. Power Electron., vol. 31, no. 8, pp. 5967-5973, Aug. 2016.

[15] S. S. Lee and K. Lee, "Dual-T-Type 7-Level Boost Active-Neutral-PointClamped (DTT-7L-BANPC) Inverter," IEEE Trans. Power Electron.,vol. 34, no. 7, pp. 6031-6035, July 2019.

[16] Y. P. Siwakoti, A. Mahajan, D. J. Rogers and F. Blaabjerg, "A Novel Seven-Level Active Neutral-Point-Clamped Converter With Reduced Active Switching Devices and DC-Link Voltage," IEEE Trans. Power Electron., vol. 34, no. 11, pp. 10492-10508, Nov. 2019.

A Cascaded Flying Capacitor Multilevel Inverter with Double-Boost Voltage Gain and reduced capacitor count for solar PV systems

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***Abstract*—Fed by a mass of photovoltaic (PV) panels in series, the traditional buck-type flying-capacitor (FC) multilevel inverter has poor operational reliability in grid-connection application. In order to obtain a step-up output voltage, a novel five-level voltage source inverter is proposed by cascading two FC cells. The proposed inverter reduces the number of capacitors compared to the traditional buck-type topology with the same number of voltage levels. Moreover, the voltages of the capacitors can be self-balanced without using any other active-balancing strategies. Descriptions and theoretical analyses of the proposed inverter are given, followed by simulation results verifying its feasibility.**

Keywords—Power converter, switched-capacitor, flying-capacitor, multilevel inverter

I. Introduction

The ever-growing PV distributed generation has given birth to various power converters/inverters to couple the PV modules to the ac mains [1]. During this process, the leakage current induced by the parasitic capacitance between the PV arrays and the ground needs to be suppressed. And the use of multilevel inverters has been demonstrated as an appealing method [2]. Compared to the two-level VSI, the three-level VSI improves the quality of the output voltage with low total harmonic distortion (THD). Meanwhile, the voltage stresses on the power switches are reduced, which facilitates the utilization of low-voltage devices.

In general, the traditional MLIs can be divided into three groups including the diode-clamped or neutral-point-clamped (NPC) MLI, the capacitor-clamped or flying-capacitor (FC) MLIs, and the cascaded-full-bridge (CHB) MLIs. Among various multilevel inverter topologies, the FC multilevel inverter is regarded as a good candidate due to its inherent capacitor voltage balancing (Fig. 1(a)) [3]. However, FC multilevel inverter may use more capacitors, some of which are with voltages higher than the peak value of the ac output. Furthermore, the step-down feature is not suitable for the grid-connection application, since the output voltages of the PV panels are relatively low (mostly less than 100 V). Therefore, as a grid inverter, it needs to boost the source-voltage to the predefined grid voltages (110 V or 220 V rms) [4]–[6]. Otherwise, the input of the grid inverter requires a number of PV modules connected in series, which increases the burden of maximum power point tracking and reduces the operational reliability.

In this work, a novel five-level inverter is proposed by cascading two FC cells as shown in Fig. 1(b). The proposed inverter has the following features.

- The boosted output voltage is achieved with a voltage gain of two.
- The number of capacitors is reduced without using high voltage-rating capacitors.
- The voltages of the capacitors can be self-balanced.

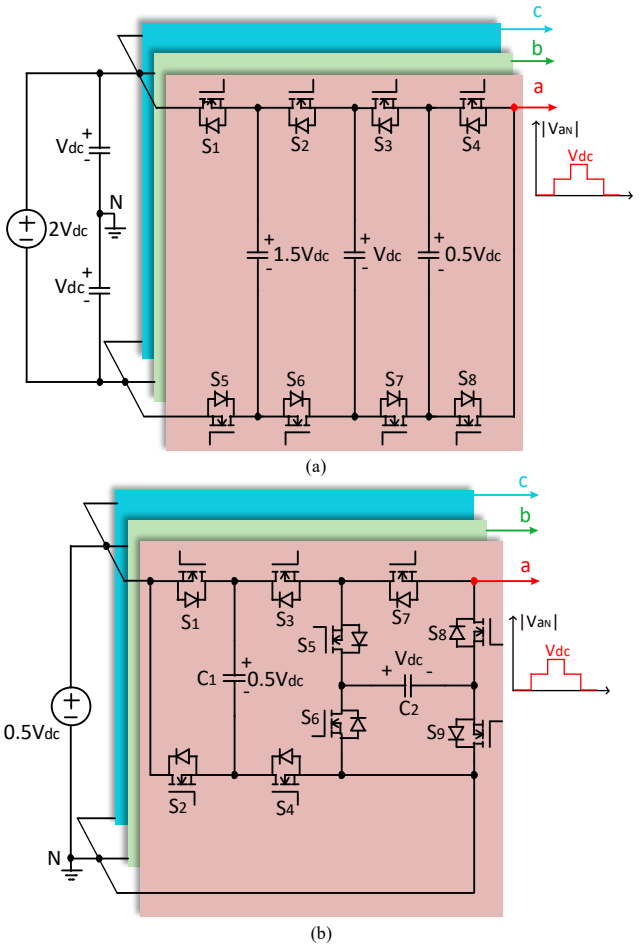

Fig. 1. Topologies of the (a) traditional FC buck-type five-level inverter [3] and (b) the proposed FC boost-type five-level inverter, both with maximum $V_{aN} = V_{dc}$.

For simplicity, only a single phase-leg is considered as shown in Fig. 2 and will be subsequently analyzed. As can be seen, the ac output and the DC input are commonly grounded which means the leakage current can be effectively suppressed for the PV systems.

II. Operating Mechanism Of The Proposed Inverter

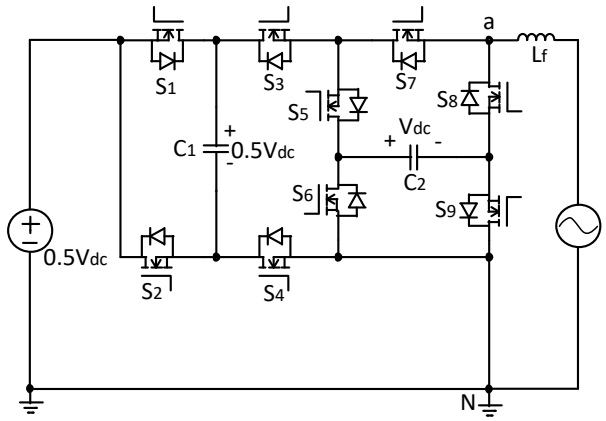

Fig. 2. Single-phase configuration of the proposed inverter.

The proposed five-level inverter has six operating states as depicted in Fig. 3. Although MOSFETs are used to represent the power switches, they can also be replaced by IGBTs, each anti-parallel connected with a diode. It should be mentioned that the proposed inverter can operate under any power factor, but for PV applications, the unity power factor is usually considered.

In State I (Fig. 3(a)), the switches S_2, S_3, S_5, S_7, and S_9 are turned on. The dc source in series connected with capacitor C_1 discharges to the capacitor C_2, which is supplying the ac output ($V_{aN} = V_{dc}$). In State II (Fig. 3(b)), the switches S_1, S_3, S_4, S_7, and S_9 are turned on. The dc source discharges to the capacitor C_1, which is feeding the ac output ($V_{aN} = 0.5V_{dc}$). In State III (Fig. 3(c)), the switches S_1, S_3, S_4, S_8, and S_9 are turned on. The dc source discharges to the capacitor C_1. The ac output is in the null (zero) state ($V_{aN} = 0$). In State IV (Fig. 3(d)), the switches S_2, S_3, S_5, S_8, and S_9 are turned on. The dc source in series connected with capacitor C_1 discharges to the capacitor C_2. The ac output is also in the null state. In State V (Fig. 3(e)), the switches S_1, S_3, S_5, and S_8 are turned on. The capacitor

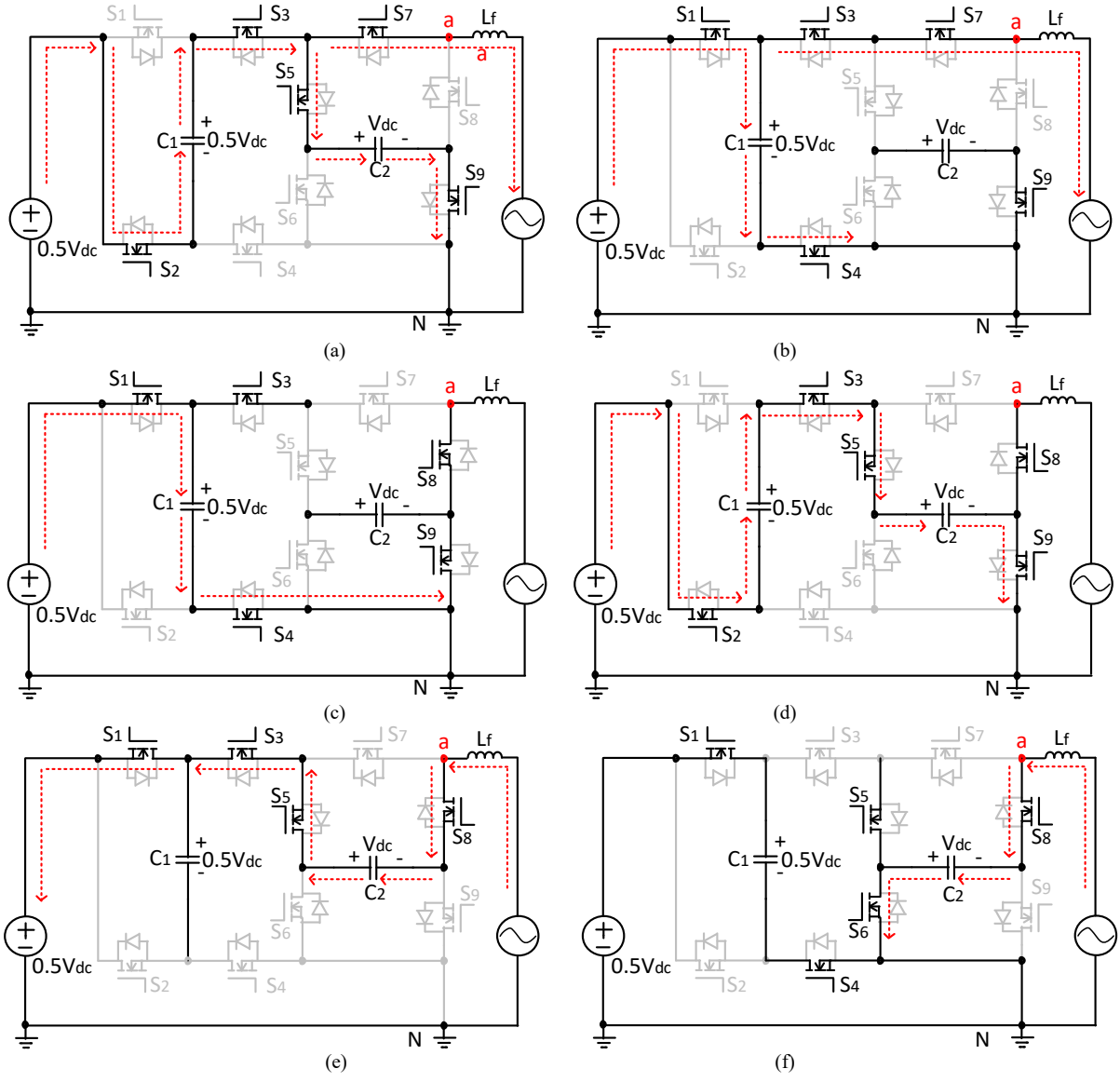

Fig. 3. Operating states with AC output voltage (a) $V_{aN} = V_{dc}$, (b) $V_{aN} = 0.5V_{dc}$, (c)-(d) $V_{aN} = 0$, (e) $V_{aN} = -0.5V_{dc}$, and (f) $V_{aN} = -V_{dc}$ (red dashed line represents the current flowing path).

TABLE I. OPERATING STATES OF THE CAPACITORS

	States	V_{aN}	C_1	V_{C1}	C_2	V_{C2}
A_1	I	V_{dc}	Dis.	↓	Ch.	↑
	1↓ 1↓					
	II	$0.5V_{dc}$	Ch.	↑	X	—
A_2	II	$0.5V_{dc}$	Ch.	↑	X	—
	1↓ 1↓					
	III/IV	0	Ch. or Dis.	↑ or ↓	X or Ch.	— or ↑
A_3	III/IV	0	Ch. or Dis.	↑ or ↓	X or Ch.	— or ↑
	1↓ 1↓					
	V	$-0.5V_{dc}$	X	—	Dis.	↓
A_4	V	$-0.5V_{dc}$	X	—	Dis.	↓
	1↓ 1↓					
	VI	$-V_{dc}$	Ch.	↑	Dis.	↓

C_2 anti-series connected with dc source discharges to the output ($V_{aN} = -0.5V_{dc}$). In State VI (Fig. 3(f)), the switches S_1, S_4, S_5, S_6, and S_8 are turned on. The capacitor C_2 discharges to the output ($V_{aN} = -0.5V_{dc}$).

Multicarrier modulation (Fig. 4) can be used to generate the above six states for the proposed inverter. There are only two operating states in each carrier band. For example, when carrier A_1 is enforced, operation only includes states I-II, with output voltage transiting between V_{dc} and $0.5V_{dc}$, respectively.

In each carrier band (A1-A4), the capacitors may be charged (Ch.), discharged (Dis.) or in idle (X) state. Accordingly, the capacitor voltages may increase (↑), decrease (↓), or keep constant (—) as shown in Table I.

III. THEORETICAL ANALYSIS

The voltage gain of the proposed inverter can be expressed as

$$G = \frac{V_{aN\_max}}{V_{in}} = \frac{V_{dc}}{0.5V_{dc}} = 2 \quad (1)$$

where V_{aN_max} is the maximum output voltage and V_{in} is the dc input source-voltage.

From Fig. 3(a)-(f), the voltages across the power switches when they are off can be found and their relationships are expressed as

$$V_{ds1} = V_{ds2} = V_{ds3} = V_{ds4} = V_{ds5} = 0.5V_{dc} \quad (2)$$

$$V_{ds6} = V_{ds7} = V_{ds8} = V_{ds9} = V_{dc} \quad (3)$$

It can be seen that the voltage stresses (blocking voltage) of the power switches are V_{aN_max} or $0.5V_{aN\_max}$. Moreover, the voltages across the capacitors C_1 and C_2 are $0.5V_{aN\_max}$ and V_{aN_max}, respectively, which means lower voltage rating capacitors can be selected compared to the traditional FC buck-type inverter (Fig. 1 (a)).

Table I also shows that both V_{C1} and V_{C2} can be self-balanced, since two or more charging states for the

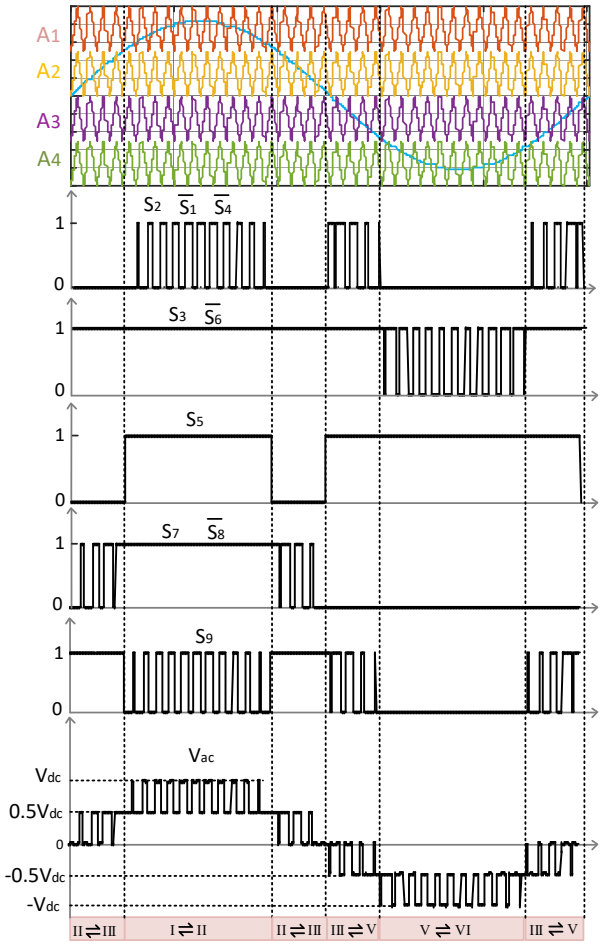

Fig. 4. Multicarrier modulation strategy (state III is selected to generate $V_{aN} = 0$ here).

capacitors can be found. However, one can find that the voltage V_{C2} consistently drops during carrier band A_4, because it discharges to the output in states V-VI. Therefore, C_2 should have relatively large capacitance to hold the capacitor voltage V_{C2}. Assume that the voltage ripple (ΔV_{C2}) is less than $1\%V_{aN\_max}$, the following equation can be written

$$\frac{\Delta V_{C2}}{V_{a\_max}} = \frac{1}{V_{a\_max}C_2}\int_{t_1}^{t_2} i_o(t)$$

which can be rewritten as

$$\frac{M_{ac}}{C_2 R}\int_{t_1}^{t_2} sin(\omega t) \le \frac{1}{100} \quad (4)$$

where $i_o(t)$ is the ac output current and also the capacitor-discharge current of C_2 during States V-VI; R is the load resistance and M_{ac} is the modulation index of the sinusoidal reference ($M_{ac} > 0.5$).

By letting $M_{ac}\sin(\omega t) = 0.5$, the time t_1 can be found by

$$t_1 = \frac{1}{\omega} sin^{-1}\left(\frac{0.5}{M_{ac}}\right) \quad (5)$$

where ω is the angle frequency of the ac output. For t_2, it can be calculated according to periodicity

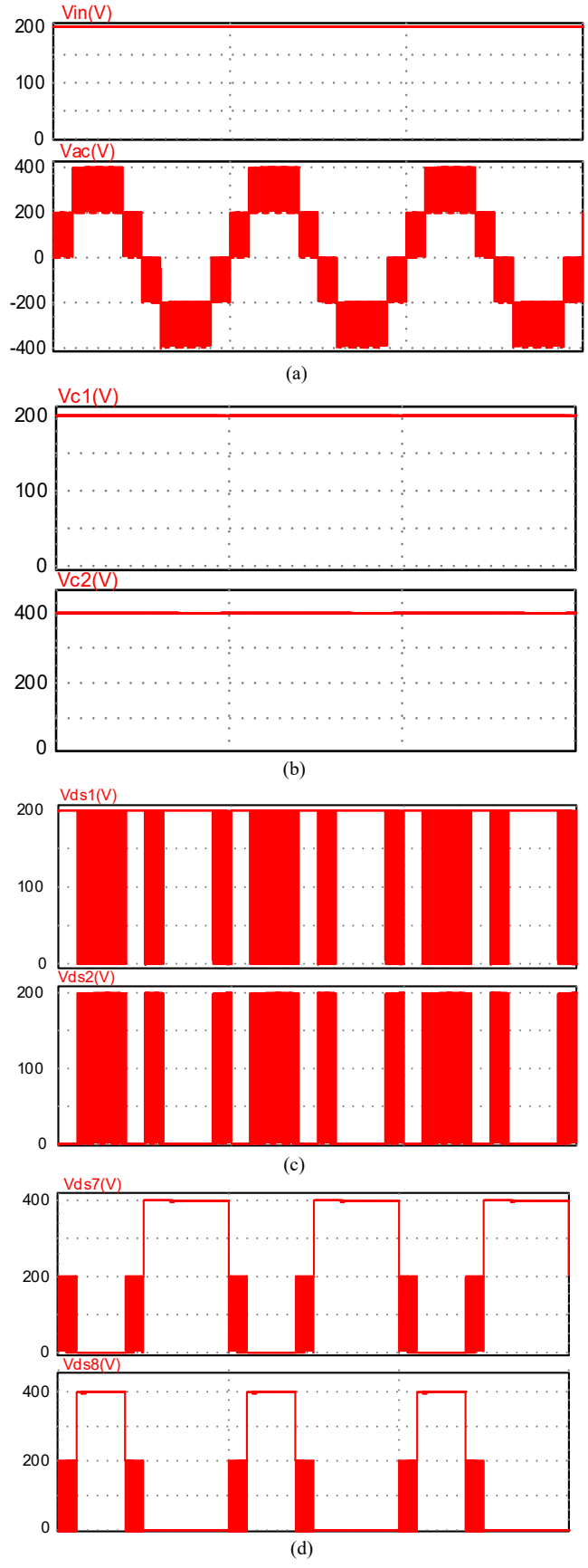

Fig. 5. Key voltages of simulation results including (a) V_{aN}, V_{in}; (b) V_{C1}, V_{C2}; (c) V_{ds1},V_{ds2}; (d) V_{ds7}, V_{ds8}.

$$t_2 = \frac{\pi}{\omega} - t_1 \tag{6}$$

Using (4)-(6), the capacitance of C_2 can be found as

$$C_2 \geq \frac{100M_{ac}[\cos(\omega t_2) - \cos(\omega t_1)]}{R\omega} \tag{7}$$

The equation in (7) suggests that the capacitor size would be inversely proportional to the fundamental output frequency and loading resistance.

IV. Simulation Results

The proposed inverter has been simulated with the following parameters, and the simulation results are shown in Fig. 5 (a)-(d). The input voltage ($\boldsymbol{V_{in}}$) was $\boldsymbol{200\,V}$ ($\boldsymbol{V_{dc}} = \boldsymbol{400\,V}$), and the nominal output power was $\boldsymbol{1\,kW}$. Switching frequency for the power switches was set to $\boldsymbol{f_s = 50\,kHz}$. The selected capacitances were $\boldsymbol{C_1 = 200\,\mu F}$ and $\boldsymbol{C_2} = \boldsymbol{4000\,\mu F}$, respectively. Simulation results show that two times of voltage gain is achieved. A five-level ac output with a maximum voltage of 400 V (Fig. 5(a)) was generated. The capacitor voltages, V_{C1} and V_{C2} are depicted in Fig. 5 (b). With the aforementioned parameters, the voltage across the capacitors were self-balanced to stable values of approximately $0.5V_{dc}$ and V_{dc}. The blocking voltages for some of the switches $\boldsymbol{S_1}$- $\boldsymbol{S_2}$ and $\boldsymbol{S_7}$- $\boldsymbol{S_8}$ are shown in Fig. 5 (c)-(d). Their values were $0.5V_{dc}$ and V_{dc}, which match the calculations in (2)-(3).

V. Conclusion

A novel five-level voltage source inverter is proposed by cascading two FC cells. Twofold voltage gain is achieved by only using two capacitors, whose voltage-ratings are relatively low. Furthermore, the voltages of the capacitors can be self-balanced, which means no active-balancing circuits are required. Some simulated results initially verify its feasibility in this digest. More details are to be presented in the final paper. It is expected that the proposed multilevel inverter is suitable for renewable energy applications where boosted ac voltages are required.

References

[1] J. Yan, Y. Yang, P. E. Campana, and J. He, "City-level analysis of subsidy-free solar photovoltaic electricity price, profits and grid parity in China," *Nature Energy*, vol. 4, pp. 709-717, Aug., 2019

[2] A. Kadam and A. Shukla, "A Multilevel Transformerless Inverter Employing Ground Connection Between PV Negative Terminal and Grid Neutral Point," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8897-8907, Nov. 2017.

[3] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu and S. Jain, "Multilevel Inverter Topologies with Reduced Device Count: A Review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135-151, Jan. 2016.D. Meneses,

[4] F. Blaabjerg, Ó. García and J. A. Cobos, "Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649-2663, Jun. 2013.

[5] M. Chen, P. C. Loh, Y. Yang and F. Blaabjerg, "A Six-Switch Seven-Level Triple-Boost Inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1225-1230, Feb. 2021.

[6] M. Chen, C. Yin and P. C. Loh, "Magnetically Coupled High-Voltage-Boost Split Y-Source Inverter Without Leakage-Induced Voltage Spikes," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5444-5455, July 2020.

Coupling Tracking and Control in the Dynamic Wireless Charging for Electric Vehicles

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Abstract: In the wireless charging for the moving electric vehicles (EVs), the unstable coupling that largely influences the output robustness is brought by the dynamic manner. In this paper, a control scheme based on a simple LC compensated dynamic wireless charging couplers is proposed, where the exact mutual inductance is extracted by monitoring the direct current (dc) current and voltage outputs. The maximum total efficiency is thus achieved by adjusting the voltage inputs for the transmitters (Txs). A 200mm*100mm Tx array is modeled, and the overlap area is 50% of the size in the simulation and experiment. The performance of the control strategy is proved by the experimental results, and the efficiency could be universally improved by 2.1%~5.2%.

Keywords: wireless charging; mutual inductance extraction, maximum efficiency, control strategy

I. Introduction

Dynamic wireless charging allows the electric vehicles freely move on the transmitter array while there is little interruption to power transfer [1-2]. However, the power output is frequently disturbing due to the coupling between the Txs and Rx is varying with car movement.

The goals of a well-established dynamic charging system are satisfied stability and maximum total efficiency. The maximum energy efficiency transfer (MEET) is achieved by finding the optimized ratio of primary currents in Txs [3]. The currents of each Tx coil are synchronously adjusted so that the reflected impedance of Rx is the optimized load impedance.

The MEET has been established for multi-Tx charging system by many research forces, and the requirements could be concluded as following:
a) The ratio of the primary currents should be found by $I_{P1}:I_{P2}:I_{P3}:...:I_{Pn}=M_{1S}:M_{2S}:M_{3S}:...:M_{nS}$, where the M_{nS} is the mutual inductance between Tx_n and Rx
b) The speed of tracking must be fast enough to calibrate the mutual inductance and the real-time control output

There are many methods to perform MEET in different environments. The most simple and robust way is the perturb and observe (P&O). The variation of the mutual inductance is not necessarily found in this method, however, the real-time output voltage and current are sensed to calculate the system efficiency. The secondary side of wireless power transfer (WPT) system is linked to a dc/dc buck-boost converter, which is applied for adjusting the load impedance [4-5]. However, the P&O method relies badly on the iteration process, where the optimum load is usually converged after seconds delay [6].

Linear control algorithms are thus proposed to overcome the delay. The better run time performance is realized by integrating proportion integral (PI) control [7]. The error between reference maximum voltage gain and real value is detected as the input of PI controller. The limitation of linear control is that the error cannot be found in LCC resonant inverter due to its constant current property [8].

A straight way of tracking the maximum power efficiency is to find the exact mutual inductance. By sensing the impedance and voltage, it is possible to extract coupling coefficient precisely [9-10]. In the control strategy introduced in [11], the first step is to reveal the initial mutual inductance, and the second step is to estimate the latest coupling. This method is rather simple because the resonant current is not measured, nevertheless, it still has large delay of a few hundred milliseconds.

Based on the reviewof aforementioned references, few of them are developed based on a multiple Txs system, which is the practical model of dynamic charging. In addition, the control delays of some methods is too large to be used in charging EVs. To achieve better real time performance, a control scheme based on the extracted mutual inductance is proposed in this paper, where only dc real time values are needed. The relation between the optimum load impedance and the input voltage of each Tx is established. In section II, a 3 Txs and 1 Rx (3-to-1) charging system is modeled, which is regarded as the vehicle motion when drive over the power array. Then, the mutual inductance ratio and exact values are calculated under certain proper assumption. The control scheme is proposed in section III, where the optimum voltage is derived. In section IV, the simulation and experiments are proceed so that the stability of the output and total efficiency are proved to be improved.

II. Modelling and Control Strategy

2.1 System model

The dynamic charging system consists of DC voltage inputs, bridge inverters, Tx array and a receiver. In this paper, the 3 Txs and 1 Rx (3-to-1) model is adopted in all analysis.

The basic construction is demonstrated in Fig.1. Besides the electronic components, the mutual inductance among Txs and Rx is marked. Differed from 1-to-1 charging, there are multiple couplings that could influence the behavior in the same time. Among them, M_{1S}, M_{2S} and M_{3S} significantly contribute to the transferred power and efficiency. Hence, for easy analysis, it can be assumed that the mutual inductance among Txs (M_{12}, M_{13}, M_{23}) is neglected. The weak coupling M_{kS} would bring lower efficiency, and thus the power input of this winding should be adjusted to a lower level so as to avoid producing exceeded reactive power. The voltage of the winding $U_{in,k}$ should be frequently controlled after its relation

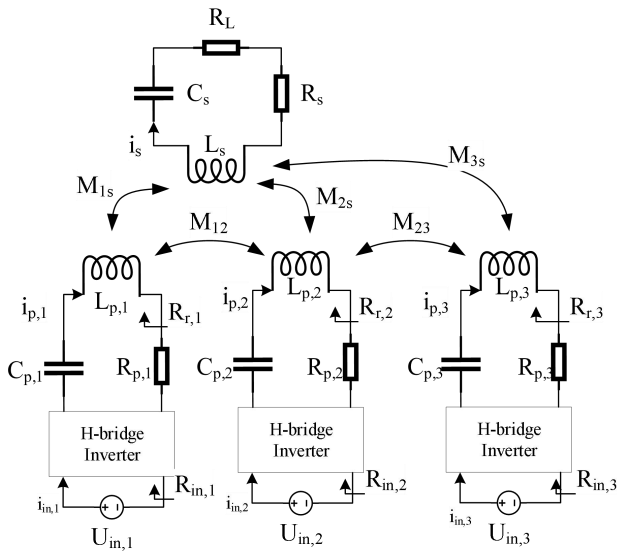


Fig. 1: System model of 3-to-1 dynamic wireless charging

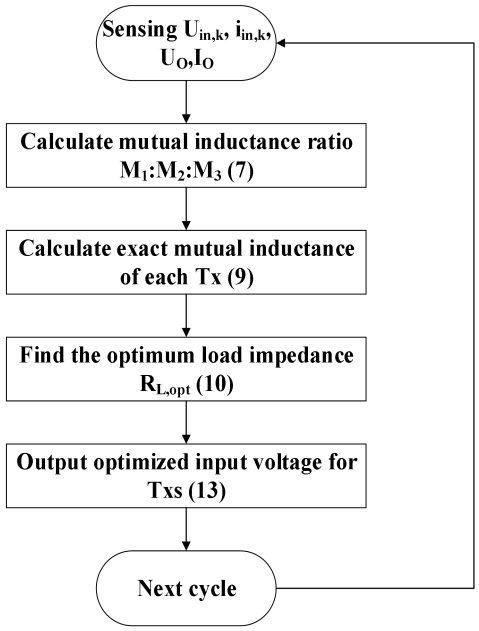


Fig.2: Control scheme flowchart

with mutual inductance is precisely found.

2.2 The extraction of mutual inductance ratio

Inheriting the equivalent circuit shown in Fig. 1, the ac voltage inputs and secondary side current can be calculated by Kirchhoff Voltage Law (KVL) in (1).

$$\begin{pmatrix} U_{in,a} \\ U_{in,b} \\ U_{in,3} \\ 0 \end{pmatrix} = \begin{pmatrix} Z_{P,1} & j\omega M_{12} & j\omega M_{13} & j\omega M_{1S} \\ j\omega M_{12} & Z_{P,2} & j\omega M_{23} & j\omega M_{2S} \\ j\omega M_{13} & j\omega M_{23} & Z_{P,3} & j\omega M_{3S} \\ j\omega M_{1S} & j\omega M_{2S} & j\omega M_{3S} & Z_S + R_L \end{pmatrix} \begin{pmatrix} i_{P,1} \\ i_{P,2} \\ i_{P,3} \\ i_S \end{pmatrix} \quad (1)$$

where

$$Z_{P,k} = \frac{1}{j\omega C_{P,k}} + j\omega L_{P,k} + R_{P,k} \quad (2)$$

$$Z_S = \frac{1}{j\omega C_S} + j\omega L_S + R_S \quad (3)$$

The reflected voltage, which is also the voltage of the Tx inductors, is

$$U_{r,k} = j\omega M_{kS} i_S \quad (4)$$

Hence, the reflected resistance can be calculated as following equation (5).

$$R_{r,k} = \frac{U_{r,k}}{i_{P,k}} j\omega M_{kS} i_S = j\omega M_{kS} \frac{i_S}{i_{P,k}} \quad (5)$$

The reflected resistance is an ac resistance and cannot be measured directly, but the relation with the input equivalent resistance could be found as (6).

$$R_{r,k} = \frac{\pi^2}{8} R_{in,k} - R_{P,k} \quad (6)$$

Consequently, the ratio of the mutual inductance could be expressed as the division of reflected resistance and the input voltage.

$$\frac{M_{aS}}{M_{bS}} = \frac{\left(\pi^2 R_{in,a}/8 - R_P\right) R_{in,b}}{\left(\pi^2 R_{in,b}/8 - R_P\right) R_{in,a}} \frac{U_{in,a}}{U_{in,b}} \quad (7)$$

The $i_{in,k}$ and $U_{in,k}$ can be easily obtained by the micro-controller, and the ratio can be calculated in dc observed values. The equation (7) is important because the ratio is not only used to indicate the input power, but also needed to acquire exact value of each mutual inductance.

Table 1 Key parameters of the experiment setup

Parameter	Value	Parameter	Value
L_P	25μH	L_S	25μH
C_P	5.6μF	C_S	5.6μF
R_P	0.312Ω	R_S	0.325Ω
U_{in}	10V	R_L	5Ω

2.3 Calculation of exact mutual inductance

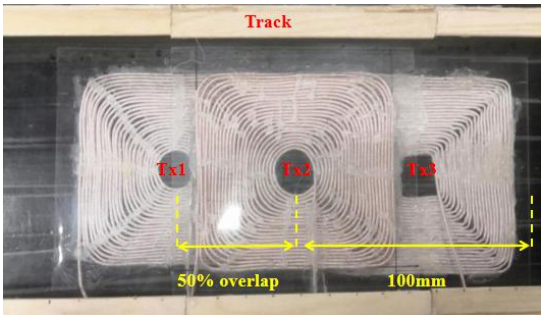
The receiver output voltage UO is

$$U_O = \frac{\pi^2}{4} \frac{\omega R_L}{R_S + R_L} \sum_{n=1}^{3} (M_{nS} i_{P,n}) \quad (8)$$

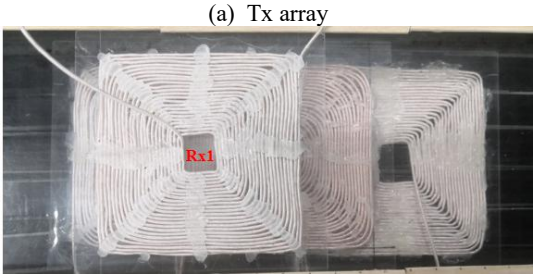
Due to the primary current fulfill the assumption I_{P1}:I_{P2}:I_{P3}:...:I_{Pn}=M_{1S}:M_{2S}:M_{3S}:...:M_{nS}, the exact mutual inductance M_{kS} is written as

$$M_{kS} = \frac{4U_O\left(R_S + R_L\right)}{\pi^2 \omega R_L \left(\frac{1}{2} i_{in,k} + \frac{1}{2} \sum_{n=1, n\neq k}^{3} \frac{M_{nS}}{M_{kS}} i_{in,n}\right)} \quad (9)$$

The ration M_{nS}/M_{kS} can be obtained by equation (7), and the current $i_{in,n}$ and U_O are dc quantity that could be directly monitored.



(a) Tx array



(b) Rx and Txs

Fig.3:Experiment Platform

2.4 Optimized voltage input based on load impedance

The reflected load of secondary sides is shifting unceasingly due to the vehicles motion. Therefore, the optimized impedance of the load is not constant. According to the maximum total efficiency, the optimum load resistance could be written as

$$R_{L,opt} = R_S \sqrt{1 + \frac{\omega^2 \sum_{n=1}^{3} M_{nS}^2}{R_P R_S}} \tag{10}$$

From the voltage conversion of the full-bridge diode converter, the optimum output voltage is

$$U_{O,opt} = \sqrt{R_{L,opt} U_O I_O} \tag{11}$$

The ac current goes through the Tx could be expressed as

$$i_{P,k,opt} = \frac{4}{\pi^2} \frac{M_{kS}\left(\frac{R_S}{R_{L,opt}} + 1\right)}{\omega \sum_{n=1}^{3} M_{nS}^2} \sqrt{R_{L,opt} U_O I_O}) \tag{12}$$

The optimum input voltage is the multiplication of equivalent $i_{p,k,opt}$ and input resistance $R_{in,k}$.

$$U_{in,k,opt} = \frac{\pi^2}{4} i_{P,k,opt} \left(\frac{\omega^2 \sum_{n=1}^{3} M_n^2}{R_S + R_{L,opt}} + R_P \right) \tag{13}$$

2.5 Control scheme and indications

From the previous derivation of the optimum voltage, the real-time primary inputs and load outputs should be continuously monitored during the time. The control logic and the cycle loop is demonstrated in Fig. 2. After sensing the feedback of U_{in} and i_{in}, the ratio of mutual inductance can be

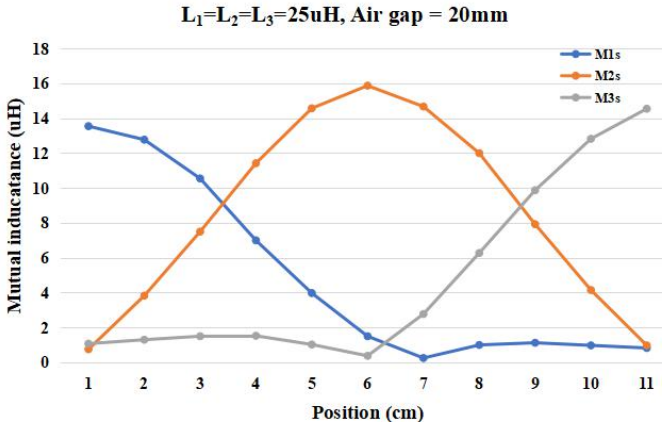


Fig.4: Mutual inductance between Txs and Rx with motion position

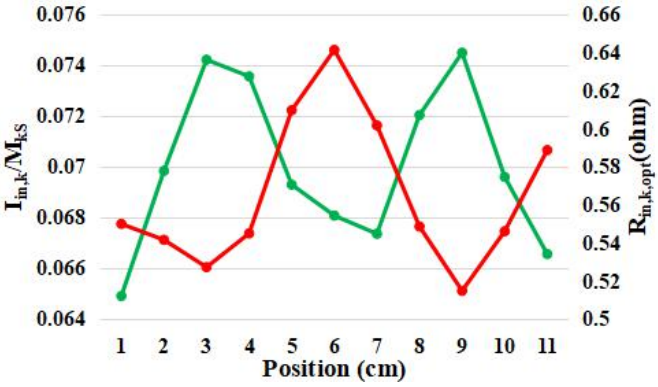


Fig.5: The proportional factor $i_{in,k}/M_{kS}$ and the optimum load impedance

calculated by using equation (7). And the exact mutual inductance is yielded in equation (9). The optimum input voltage $U_{in,k,opt}$ for each Tx is obtained by integrating the expected load impedance.

III. Simulation and Experiment Results

3.1 Experiment setup

The Tx and Rx are both designed as the same size of 100mm*100mm, 25 turns. Hence, they share the similar inductance as 25μH. The prototype is also reduced to a smaller scale proportionally, where the air gap is set to be 20mm. The switching frequency of the inverter is 20kHz, and this is also inherited for the design of the resonant circuit. To neutralizing higher order harmonic distortion when the Rx is fully alignment to one Tx, the compensated capacitance is chosen as 5.6μF. The copper wire resistance in the inductance are measured to be 0.3Ω for each coil. The key parameters of the setup are listed in Table I.

The three Txs are placed as 50% overlapped to each other, as demonstrated in Fig. 3. The Rx is regulated by a wooden track where only horizontal movement are allowed. It simulated the driving manner of a EV without vertical vibration.

3.2 Experiment results

The horizontal range is 200mm, so the measurement of mutual inductance are divided into 11 sampling points (in 10mm interval). The mutual inductance between each Tx and Rx are shown in Fig. 3. After integrating the results into PSIM simulation , the proportional factor $i_{in,k}/M_{kS}$ can be subsequently calculated, and the optimized load resistance are also derived. As can be seen in Fig. 4, the aforementioned factor is reverse proportional to the optimized resistance. It means that the power input of the Tx should be adjusted to a lower level when its coupling with Rx is weak. The controlled

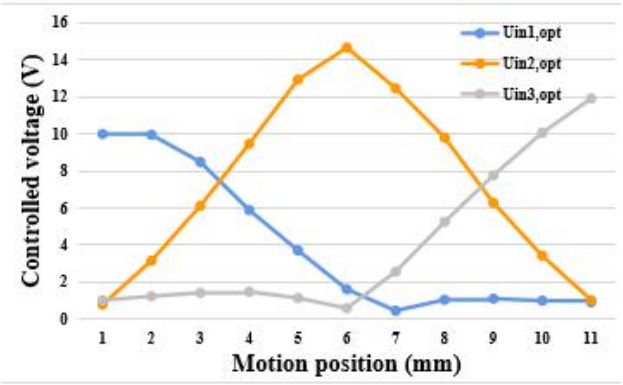


Fig.6: Voltage for each Tx after control

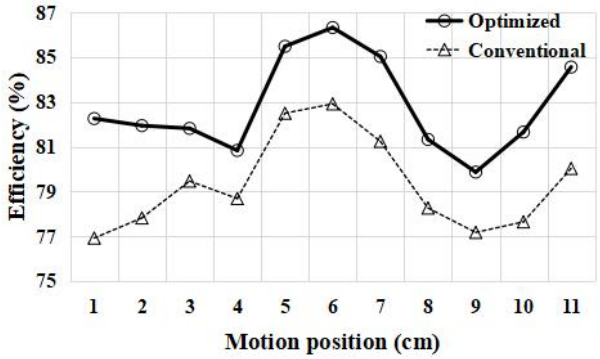


Fig.7: Total efficiency with optimized voltage inputs

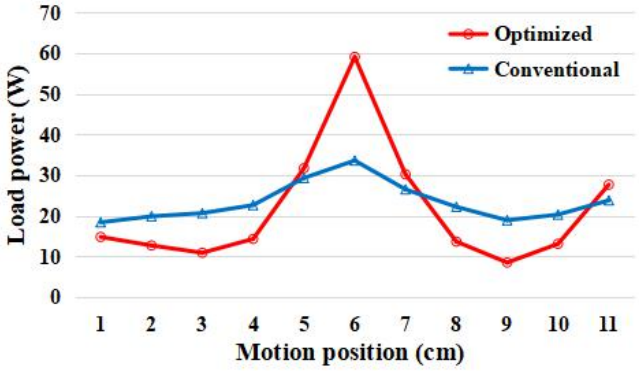


Fig.8: Load power after optimization

voltage for Tx windings are depicted in Fig. 6.

The total efficiency in each sampling points before and after optimization is shown in Fig. 7. The waveform in dash line is the efficiency by applying the same voltage input to Txs, and the waveform in solid line is the one of adopting the proposed control scheme. The trend of the total efficiency follows the variation of mutual inductance. As can be concluded in Fig. 7, the total efficiency is improved universally in all movement range, and the raise can be up to 5.2% when the coupling is stronger.

3.3 Discussions

For a series-series LC resonant compensation, the compensation capacitance is unchangeable once the design process is finished. Despite of the capacitor is compensated the leakage when the Tx and Rx are fully aligned, the leakage inductance is still altered badly due to the movement of Rx. Hence, when the coupling is stronger, the influence brought by the mis-designed compensation is reduced and the power output could be higher than the conventional system. As drawn in Fig. 8, the coupling between Rx and Tx array is highest in point 6, and the power output has its peak in this point. But when the coupling becomes weak, the efficiency also drops rapidly. And with the control algorithm, the input voltage for one specific Tx stays at a lower level when this Tx is misalignment, so the power output is lower than the conventional system.

Therefore, this discussed explanation indicates the necessity to link a dc/dc buck-boost converter, rather than directly output the power to load. By adjusting the duty cycle of the converter, the voltage output can be controlled stably. For a dc linear load, the equivalent load impedance can be still easily calculated due to its clear relation with duty cycle. The configuration of the system can be seen in many other researches[9-12].

IV. Conclusion

A control scheme that is aimed at achieving maximum total efficiency of EV dynamic charging is proposed in this paper. The relation of coupling and circuit dc outputs are found, and the outputs are real-time monitored for calculating the Tx input voltage. By adopting this method to simple LC compensated charging charging prototype(a 3*100mm*100mm Tx array, a 100mm*100mm receiver), the power efficiency is proved to be improved up to 5.2% in experiment. However, the LC compensation is sensitive to the misalignment that causes low robustness in power output. The method to obtain a robust power for linear load is discussed.

Acknowledgments

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References

[1] Cui, Shumei, Wang, Zhiyuan, Han, Shouliang, Zhu, Chunbo, & Chan, C. C. (2019). Analysis and Design of Multiphase Receiver With Reduction of Output Fluctuation for EV Dynamic Wireless Charging System. IEEE Transactions on Power Electronics, 34(5), 4112-4124.

[2] Jeong, Seog Y, Park, Jun H, Hong, Gwang P, & Rim, Chun T. (2019). Autotuning Control System by Variation of Self-Inductance for Dynamic Wireless EV Charging With Small Air Gap. IEEE Transactions on Power Electronics, 34(6), 5165-5174.

[3] Huh, Sungryul, & Ahn, Dukju. (2018). Two-Transmitter Wireless Power Transfer with Optimal Activation and Current Selection of Transmitters. IEEE Transactions on Power Electronics, 33(6), 4957-4967.

[4] Zhong, W. X, & Hui, S. Y. R. (2015). Maximum Energy Efficiency Tracking for Wireless Power Transfer Systems. IEEE Transactions on Power Electronics, 30(7), 4025-4034.

[5] Minfan Fu, He Yin, Xinen Zhu, & Chengbin Ma. (2015). Analysis and Tracking of Optimal Load in Wireless Power Transfer Systems. IEEE Transactions on Power Electronics, 30(7), 3952-3963.

[6] Yeo, Tae-Dong, Kwon, DukSoo, Khang, Seung-Tae, & Yu, Jong-Won. (2017). Design of Maximum Efficiency Tracking Control Scheme for Closed-Loop Wireless Power Charging System Employing Series Resonant Tank. IEEE Transactions on Power Electronics, 32(1), 471-478.

[7] Huang, Zhicong, Wong, Siu-Chung, & Tse, Chi K. (2018). Control Design for Optimizing Efficiency in Inductive Power Transfer Systems. IEEE Transactions on Power Electronics, 33(5), 4523-4534.

[8] Kim, Do-Hyeon, Kim, Seongmin, Kim, Sang-Won, Moon, Jungick, Cho, Inkui, & Ahn, Dukju. (2020). Coupling Extraction and Maximum Efficiency Tracking for Multiple Concurrent Transmitters in Dynamic Wireless Charging. IEEE Transactions on Power Electronics, 35(8), 7853-7862.

[9] Jiwariyavej, Vissuta, Imura, Takehiro, & Hori, Yoichi. (2015). Coupling Coefficients Estimation of Wireless Power Transfer System via Magnetic Resonance Coupling Using Information From Either

Side of the System. IEEE Journal of Emerging and Selected Topics in Power Electronics, 3(1), 191-200.
[10] Kobayashi, Daita, Imura, Takehiro, & Hori, Yoichi. (2015). Real-time coupling coefficient estimation and maximum efficiency control on dynamic wireless power transfer for electric vehicles. 2015 IEEE PELS Workshop on Emerging Technologies: Wireless Power (2015 WoW), 1-6.
[11] Dai, Xin, Li, Xiaofei, Li, Yanling, & Hu, Aiguo Patrick. (2018). Maximum Efficiency Tracking for Wireless Power Transfer Systems With Dynamic Coupling Coefficient Estimation. IEEE Transactions on Power Electronics, 33(6), 5005-5015.
[12] Li, Hongchang, Li, Jie, Wang, Kangping, Chen, Wenjie, & Yang, Xu. (2015). A Maximum Efficiency Point Tracking Control Scheme for Wireless Power Transfer Systems Using Magnetic Resonant Coupling. IEEE Transactions on Power Electronics, 30(7), 3998-4008.

Design of Hybrid PWM Algorithm for Switched-Capacitor Multilevel Inverter Based on TMS320F28335

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Abstract –In this paper, the principle of the 7-level switched-capacitor inverter with an improved hybrid PWM strategy is presented. It only needs three carrier signals and one reference signal to synthesize output voltage, making the implementation more simplified. After that, the hardware design process is described in terms of control circuit based on TMS320F28335 floating-point digital signal processor, drive circuit and acquisition circuit. Moreover, the software design process involved in symmetrical regular sampling method and parameters of RMS voltage closed-loop control is also given in detail. Finally, the experimental results demonstrate the feasibility and high performance of the hybrid PWM strategy controlled by DSP TMS320F28335.

Keywords – Switched capacitor, multilevel inverter, TMS320F28335, hybrid PWM algorithm

I. INTRODUCTION

With many advantages of reduced dv/dt stresses, staircase output voltage waveforms and operating with lower switching frequency etc., multilevel inverters (MLI) have gradually become an important electric equipment for DC to AC power conversion in various fields [1]-[3]. Conventional MLIs are divided into three categories: neutral-point-clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). Nowadays, NPC and FC inverters have been successfully commercialized in many applications like FACTS [4], [5]. However, both of them have a common problem with using numerous clamping components to provide more output levels. In contrast, multiple isolated dc sources employed in CHB inverter can also generate more output levels, making the components reduced [6].

A common feature of these conventional MLIs has no boosting ability, so they need to connect the front-end boost circuit or transformer. In recent years, switched-capacitor (SC) MLIs have attracted more attention due to its boosting ability and self-balanced capacitor's voltages [7]-[9]. For instance, the conventional series/parallel SC circuit with single source invented by Hinago *et al.* in 2012 is capable of generating 2n+3 output levels [7], wherein n is the number of SC units. After that, many improved SC-MLIs are developed in the works, which can also generate 2n+3 output levels and have their own advantages [10]-[13]. In addition, since researchers focus on simpler structure to generate more output levels, some novel SC-MLIs are developed in the works [14]-[17]. The topology presented in [14] only involves eight transistors, two diodes and two capacitors, which can generate 7-level output voltage with triple boosting factor. As for [15]-[17], only 18 components employed in these 13-level topologies and they have six times boosting factor, making them suitable for low-voltage applications, such as motor control.

There are various modulation strategies adopted for SC-MLIs, such as near level control (NLC), the selective harmonic eliminated (SHE) and sinusoidal pulse width modulation (SPWM). The NLC is the simplest strategy and only suitable for more output levels. The SHE strategy can accurately reduce low-order harmonics but it needs to solve numerous nonlinear equations. In addition, SPWM strategy is to synthesize the output voltage by combining multi-carrier signals and sinusoidal reference signal, which makes the harmonics voltage concentrated near the inter multiples of switching frequency. Hence, the high-order harmonics can be suppressed by connecting a smaller LC filter with the load. Although the conventional SPWM strategies like level-shifted PWM (LS-PWM) and phase-shifted PWM (PS-PWM) can improve power quality, the capacitors' voltage ripple will accumulate when the capacitors discharges to the load continuously. In order to optimize the capacitors' voltage ripple, a hybrid PWM strategy combining LS-PWM and PS-PWM is adopted in the works [14], [15], making the voltage ripples of capacitors reduced effectively. Therefore smaller capacitors employed in these inverters can further improve power density.

In this paper, an improved hybrid PWM strategy is adopted to modulate the 7-level inverter proposed in [14]. Compared with the modulation strategy of [14] using four carriers, the improved hybrid PWM strategy only uses three ePWM modules of DSP to generate three carriers. So, it is more suitable for engineering applications. The proposed topology and PWM algorithm are described in Section II. After that, the implementation process of hybrid PWM algorithm based on TMS320F28335 is given in Section III. The experimental results verified the feasibility of the design in Section IV. Finally, the conclusion of this work gives in Section V.

II. TOPOLOGY AND MODULATION STRATEGY

A. Topology description

As shown in Fig. 1, the proposed inverter consists of an input dc source, a triple-mode SC unit and an inverting H-bridge S_3, S'_3, S_4, S'_4 to convert DC bus voltage V_{bus} to AC output voltage u_O. The triple-mode SC unit involves a pair of diodes D_1-D_2, a pair of capacitors C_1-C_2 and two pairs of transistors S_1-S_1', S_2-S_2'. By controlling these transistors reasonably, both C_1 and C_2 can be connected in series with the input dc source and charged to V_{dc}, respectively. They can also discharge to the load when connecting in parallel with the input dc source. So the V_{bus} has three different dc-levels that are $+V_{dc}$, $+2V_{dc}$ and $+3V_{dc}$. With the back-end H-bridge to alternate the output polarity, the proposed inverter is capable of generating 7-level output voltages that are 0, $\pm V_{dc}$, $\pm 2V_{dc}$ and $\pm 3V_{dc}$.

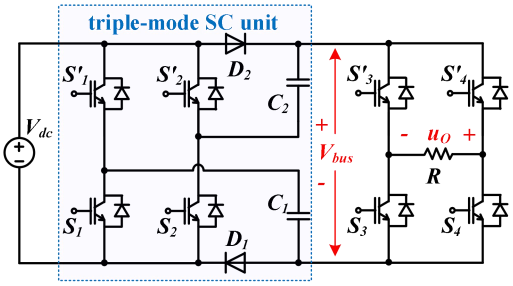

Fig.1: 7-level inverter proposed in [14].

B. Operation principle

To facilitate the analysis, the operating states of the zero and half-positive output levels are indicated in Fig. 2.

(i) State 1(u_O=+3V_{dc}): As shown in Fig. 2(a), in this operating state, the capacitors C_1 and C_2 are connected in series with the input dc source to power the load through S_1, S'_2, S_3 and S'_4. The output level is therefore +3V_{dc}.

(ii) State 2(u_O=+2V_{dc}): As shown in Fig. 2(b), the capacitors C_2 is charged to V_{dc} by the dc source through S_1 and D_2, while C_1 is connected in series with the dc source to power the load through S_1, S_3, S'_4 and D_2. In addition, as shown in Fig. 2(c), the capacitors C_1 is charged to V_{dc} by the dc source through S'_1 and D_1, while C_2 is connected in series with the dc source to power the load through S'_2, S_3, S'_4 and D_1. Therefore, the output level of Fig. 2(b) and (c) is therefore +2V_{dc}.

(iii) State 3 (u_O=+V_{dc}): As shown in Fig. 2(d), both capacitors C_1 and C_2 and dc source are connected in parallel then they are charged to V_{dc}, simultaneously. The dc source discharges to the load directly so that the output level is +V_{dc}.

(iv) State 4 (u_O=0): In this state, the transistors S_3 and S_4 or the transistors S'_3 and S'_4 are turned ON, making the zero output level generated as shown in Fig. 2(e) and (f), respectively. In addition, Both C_1 and C_2 are still charged by the dc source.

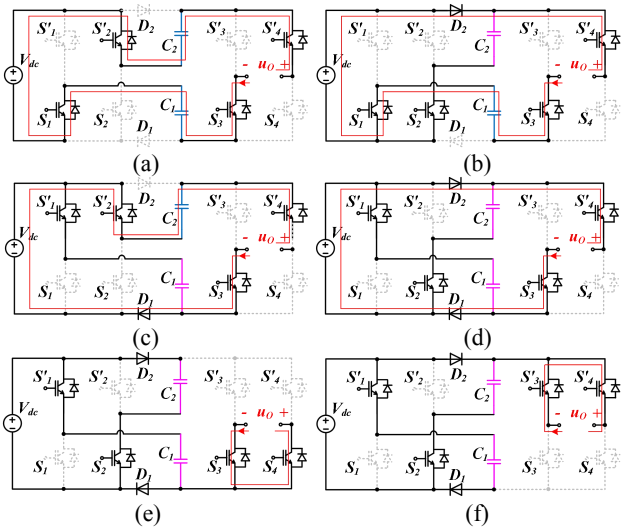

Fig.2: Operating states of zero and half-positive output levels. (a) u_O=+3V_{dc}. (b) and (c) u_O=+2V_{dc}. (c) u_O=+V_{dc}. (e) and (f) u_O=0.

By alternating the polarity of back-end H-bridge, the negative output levels are generated with the same operating states of triple-mode SC unit. Table 1 shows the operating states during one output cycle. Note that "1" and "0" represent "ON" and "OFF", respectively, while capacitors' states are noted by "▼"and "▲", which represent as discharging and charging states, respectively.

Table 1: Operating states of the proposed inverter during one output cycle

State	Capacitor's states		Switching states				u_O
	C_1	C_2	S_1	S_2	S_3	S_4	
1	▼	▼	1	0	1	0	+3V_{dc}
2	▼	▲	1	1	1	0	+2V_{dc}
	▲	▼	0	0	1	0	
3	▲	▲	0	1	1	0	+V_{dc}
4	▲	▲	0	1	0	0	0
	▲	▲	0	1	1	1	
5	▲	▲	0	1	0	1	-V_{dc}
6	▲	▼	0	0	0	1	-2V_{dc}
	▼	▲	1	1	0	1	
7	▼	▼	1	0	0	1	-3V_{dc}

C. Hybrid PWM strategy

As shown in Table 1, there are two switching states when the output levels are ±2V_{dc}, respectively. One of the capacitor is charged by the dc source, while the other discharges to the load. Taking the operating states of the half-positive cycle as an example, Fig. 3 illustrates the charging and discharging process of two capacitors between the +2V_{dc} and +3V_{dc}. It indicates that C_1 is charged from 0 to t_1 and discharges to the load from t_1 to t_2, continuously. And then it charged by the dc source again. The capacitor C_2 has the same feature as C_1. Due to its redundant states, two capacitors can be alternately charged by the dc source, making their voltage ripples reduced.

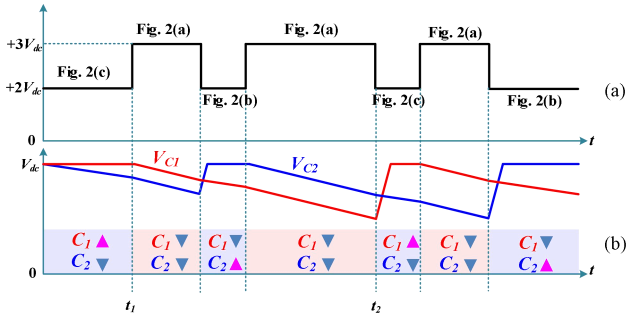

Fig.3: Operating states between +2V_{dc} and +3V_{dc} with hybrid PWM. (a) Output levels. (b) Capacitors' states.

Considering the feature of the proposed inverter, a hybrid PWM strategy combining LS-PWM and PS-PWM is adopted to modulate the proposed inverter. As shown in Fig. 4(a), all gate signals are generated by using three carrier signals u_1-u_3 and one sinusoidal reference signal u_r, where the amplitude of u_1 and u_2 is 2A_C, that of u_3 is A_C, and that of u_r is A_R. Therefore, the modulation ratio M_a can be given by

$$M_a = \frac{A_R}{3A_c} \quad (1)$$

To ensure the generation of 7-level output voltage, M_a have to satisfy the condition, i.e.

$$1 \geq M_a \geq \frac{2}{3} \quad (2)$$

Fig. 4(b) illustrates the logic circuit with the hybrid modulation. It shows that the absolute value of u_r are used to compare with u_1-u_3 for generating their original pulse

signals, while the polarity of u_r is determined by comparing with zero potential point. Combining three original pulse signals and the polarity of u_r, four gate signals V_{GS1}-V_{GS4} for eight transistors are generated.

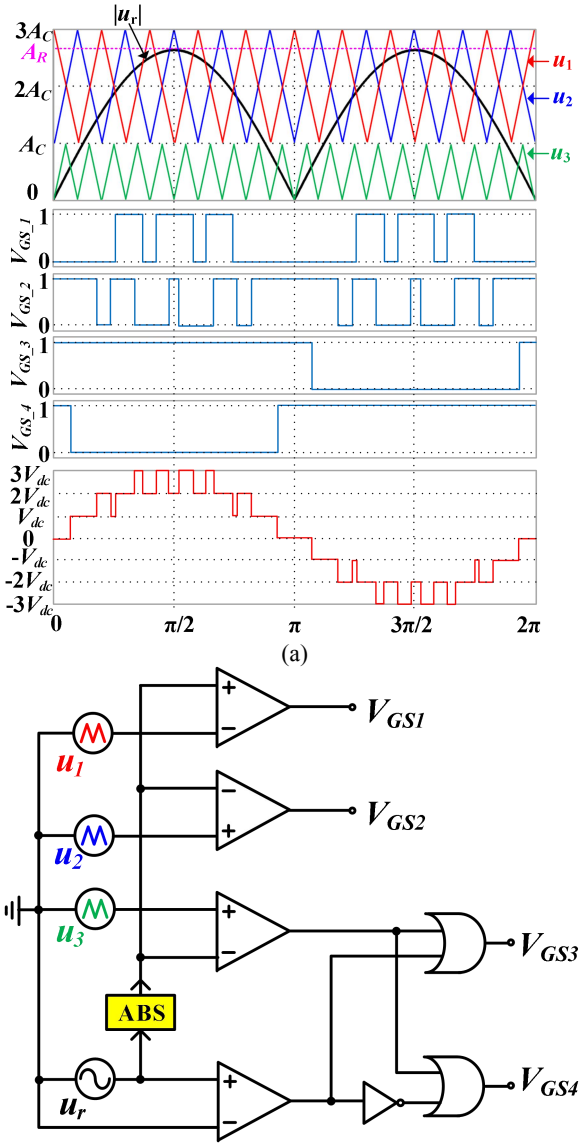

Fig.4: The proposed inverter with hybrid PWM modulation. (a) Waveforms. (b) Logic circuit of modulation.

III. Implementation Based on DSP Controller

There are many types of processors to control the switching states of the proposed inverter, such as microcontroller unit, field-programmable gate array and digital signal processor (DSP). Among them, the TMS320F28335 floating-point DSP is good at computing and generating high-frequency PWM signals. So it is adopted to implement the hybrid PWM algorithm.

As shown in Fig. 5, the system structure consists of DSP circuit, drive circuit, acquisition circuit and inverter circuit. The PWM signals generated from the DSP are amplified by the drive circuit to control the transistors of the inverter. In addition, the instantaneous output voltage measured by acquisition circuit is used for calculating the RMS of output voltage. So it can realize the RMS voltage closed-loop control by adjusting the modulation ratio.

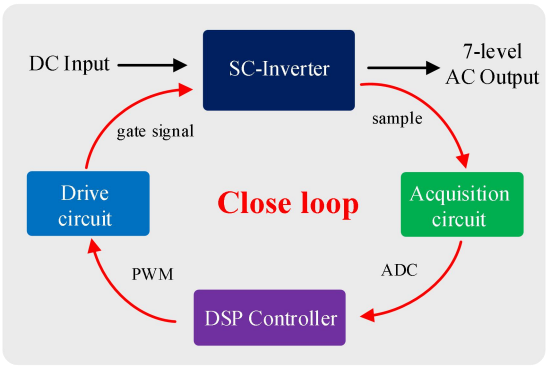

Fig.5: Control system structure.

A. DSP circuit

To implement the hybrid PWM strategy, the DSP core-board based on TMS320F28335 have been designed as shown in Fig. 6. The power supply system is composed of two low-dropout regulators that are used to convert 5V input voltage to 3.3V and 1.9V output voltages for the inner power and external power of the TMS320F28335, respectively. Since DSP TMS320F28335 has floating-point units and its main frequency is up to 150MHz, the processing speed is so fast that the ePWM module can generate high-frequency PWM signals. In addition, four 12-bit ADC modules integrated in DSP are used to convert the analog signal to the digital signal that can be processed by DSP. Normally, there are many factors that can interfere with analog signals, such as voltage spike, inrush current and switching noise. In order to protect the ADC modules, low-pass filters and surge suppression circuits are designed in this core-board.

Fig.6: DSP core-board based on TMS320F28335.

B. Drive circuit

There are two H-bridges employed in the proposed inverter as shown in Fig. 1. Therefore, the drive circuit uses IR2111 to generate both complementary gate signals with internal deadtime. Due to the IR2111 supply range from 10V to 20V, the logic input voltage is beyond the 3.3V LVTTL. To match the logic level and protect the core-board, high-speed optocouplers TLP251 are also designed in this circuit. Fig. 7 shows its schematic diagram.

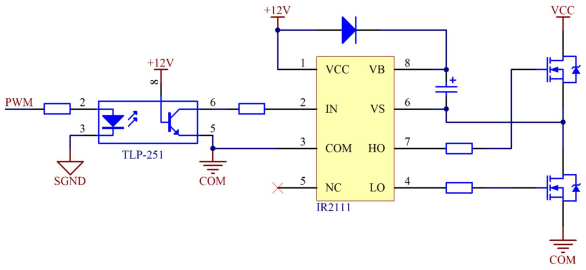

Fig.7: Schematic diagram of drive circuit.

C. Acquisition circuit

To measure instantaneous output voltage accurately, the hall-effect voltage sensor VSM025A is employed in the acquisition circuit. Since the voltage sensor requires positive-negative power and its measured signal is proportional to the output voltage, the dc-bias circuit must be adopted to make the voltage of measured analog signal between 0V and 3.3V. And therefore ADC module converts it to digital signal, correctly. The schematic diagram of acquisition circuit is shown in Fig. 8.

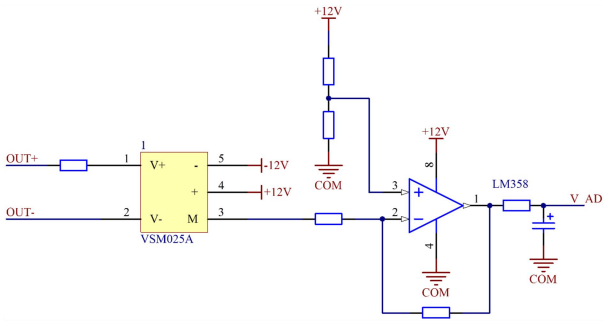

Fig.8: Schematic diagram of acquisition circuit.

D. Software design

To implement hybrid PWM algorithm in software design, the ePWM module, ADC module and PI module in DSP are programming with CCSv8. Specifically, the design process is summarized as follow steps:

Step 1: Due to less computation, symmetrical regular sampling method has been widely used for generating SPWM waveforms. It samples the amplitude of reference signal at the vertices or lowest points of the triangular carrier signal. Fig. 9 illustrates the principle of sampling process.

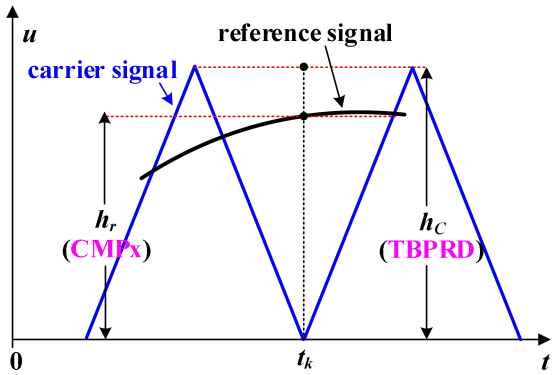

Fig.9: The principle of symmetrical regular sampling method.

At the *kth* sampling moment, it can be seen that the amplitude of carrier signal is h_C and that of reference signal is h_r. In addition, the continuous up down mode of the ePWM module gives the same symmetric carrier waveform and the TBPRD register value is proportional to h_C. Similarly, the CMPx register value is also proportional to h_r and it can therefore be calculated by

$$CMPx = \frac{h_r}{h_c} \times TBPRD \qquad (3)$$

To make the SPWM more accurate, the frequency of carrier signal must be much larger than that of reference one. Assuming that there are N_C carrier signals during one cycle of reference signal, the number of sampling values calculated from (3) is also N_C. As mentioned before, three carrier signals u_1-u_3 are used for generating original PWM signals, where u_1 and u_2 have the same frequency but the their phase difference is 180°, while the frequency of u_3 is double of them. By setting three ePWM modules, three groups of sampling values can be obtained.

Step 2: After calculating three groups of sampling values, the CMPx register value can be updated to sampling values in the interruption procedure caused by ePWM event and then three original PWM signals are generated. Except for gate signals V_{GS1} and V_{GS2}, the remaining gate signals are synthesized through logic operations as shown in Fig. 4(b).

Step 3: As mentioned before, the RMS value of output voltage is proportional to the modulation ratio M_a. So the target value of RMS voltage can be determined by that of M_a. To realize the RMS voltage closed-loop control, the acquisition circuit needs to measure N_C instantaneous values to calculate the measured RMS value during one output cycle, i.e.

$$V_{RMS} = \sqrt{\frac{\left(V_i - \frac{1}{N_C}\sum_{i=1}^{N_C} V_i\right)^2}{N_C}} \qquad (4)$$

After that, digital PI module is employed to adjust the M_a by comparing the difference between target values and measured values. Its discrete expression can be given as

$$u(k) = u(k-1) + \left(K_p + \frac{TK_p}{T_i}\right)e(k) - K_p e(k-1) \qquad (5)$$

where sample time T is consistent with time interval of interruption procedure triggered by ePWM events. In addition, the modulation ratio M_a calculated by the digital PI module is to control RMS value of output voltage during one output cycle.

To simplify the analysis, the overall flow chart of software design is shown in Fig. 10.

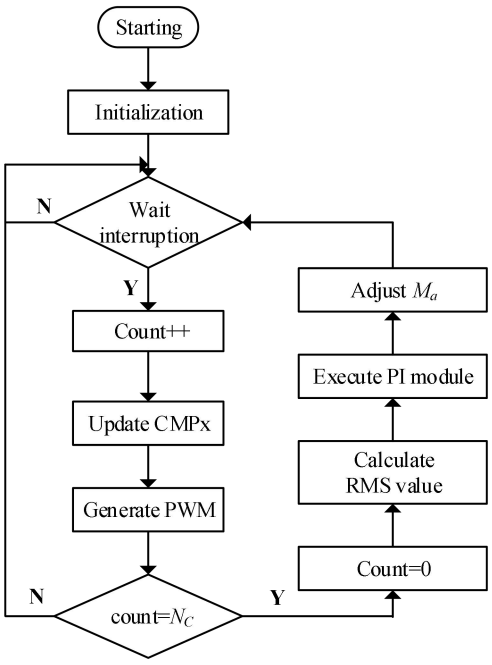

Fig.10: Flow chart of software design.

IV. Experimental Results

To verify the feasibility and high performance of the proposed inverter with hybrid modulation strategy, a 80W

experimental prototype was built by referring its specification and components in Table 2.

Table 2: Specification and components of the 7-level prototype

Input dc voltage	50VDC
Rated power	80W
Output voltage's frequency	50Hz
Switching frequency	5kHz
Capacitors C_1,C_2	1000μF
Transistors S_1,S_1',S_2,S_2'	IRFB4410PBF
Transistors S_3,S_3',S_4,S_4'	IRFB4229PBF
Half-bridge driver IC	IR2111
High-speed optocoupler	TLP251
Controller	TMS320F28335

When the M_a is set to 0.87, four gate signals for eight transistors are shown in Fig. 11, which is corresponding to the analysis in Fig. 4(a). With an inductive load 100Ω-53mH, it can also be seen that the output voltage u_O is the high-frequency seven-level SPWM waveform, while the output current i_O is very closed to sinusoidal waveform. In addition, as u_O is switched quickly between $+2V_{dc}$ and $+3V_{dc}$, the voltage of two capacitors are alternatively replenished by the dc source. Similarly, they also have the same behavior when u_O is switched quickly between $-2V_{dc}$ and $-3V_{dc}$. Therefore, two capacitors can be balanced automatically and their voltages' ripples can be reduced effectively.

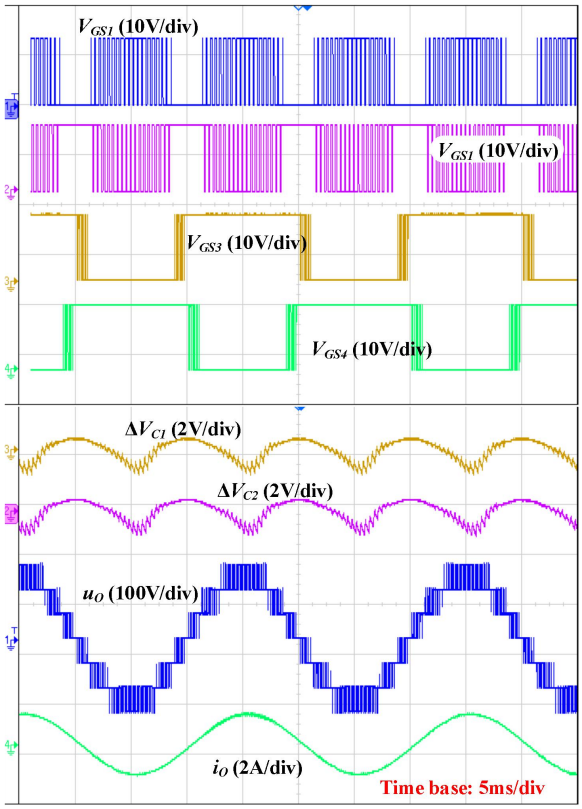

Fig.11: Experimental waveforms of an inductive load 100Ω–53mH.

To further verify the effect of reducing harmonics with the hybrid PWM algorithm, FFT analysis results in respect of output voltage and current are given in Fig. 12. It illustrates that the low-order harmonics of output voltage have been reduced by concentrating the harmonics around an integer multiple of the switching frequency. Therefore, a smaller LC filter is used for filtering out high-order harmonics. For the output current, the harmonics have been suppressed effectively by the inductive load, where the amplitude of maximum harmonics is only 7mA.

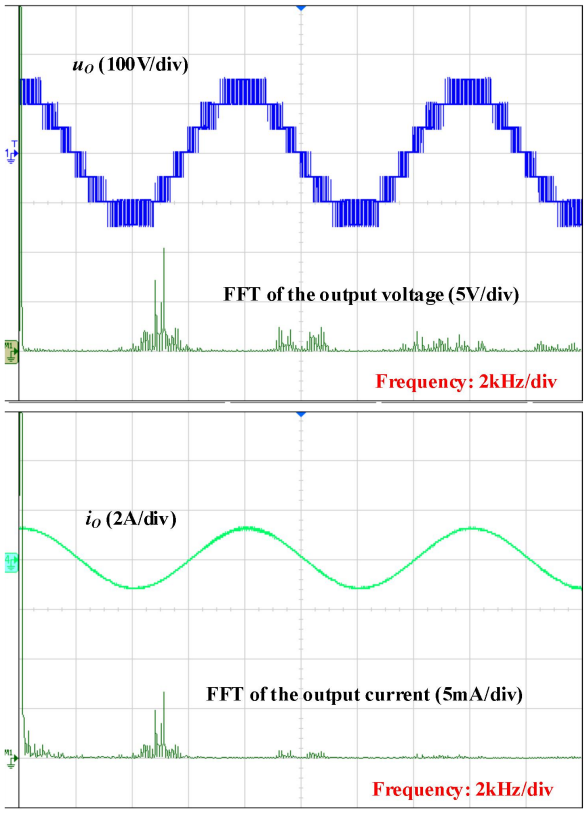

Fig.12: FFT analysis results of the output voltage and current.

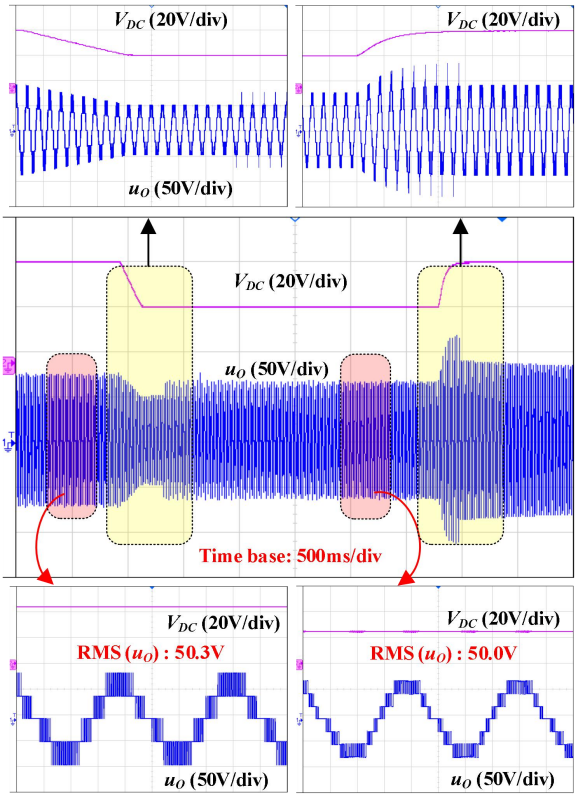

Fig.13: Experimental waveforms when the input dc voltage changes between 25V and 45V.

Fig. 13 illustrates the dynamic performance of RMS output voltage closed-loop control. Specifically, the target value of RMS voltage, K_p and T_i are set to 50V, 0.025 and 0.0075, respectively. When the input dc voltage is suddenly changed from 45V to 25V, the RMS voltage reduces accordingly but it quickly returns to the measured value 50.3V by increasing the modulation ratio M_a and remains stable. And then when the input dc voltage changes back to 45V, the RMS voltage also increases suddenly and it quickly returns to the measured value 50.0V by reducing the modulation ratio M_a. Therefore, it demonstrates that the closed-loop control for RMS output voltage has good adaptive adjustment ability.

V. Conclusion

This work analyzes the operating principle of the proposed SC-MLI with the improved hybrid PWM algorithm. With this modulation strategy, the voltages' ripples of two capacitors can be optimized, making the power density increase. In addition, the control board based on DSP TMS320F28335 is designed for implementing PWM algorithm and RMS voltage closed-loop control. The design of drive circuit, acquisition circuit and software programming is also discussed in detail. The experimental results demonstrate that the voltages' ripples of capacitors can be reduced effectively with the hybrid PWM algorithm and the digital PI controller can improve the dynamic performance.

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References

[1] J. Rodriguez, S. Bernet, B. Wu, J. Pontt and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] A. Tripathi and G. Narayanan, "Torque Ripple Minimization in Neutral-Point-Clamped Three-Level Inverter Fed Induction Motor Drives Operated at Low-Switching-Frequency," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2370–2380, May-June. 2018.

[3] R. R. Karasani, V. B. Borghate, P. M. Meshram, H. M. Suryawanshi and S. Sabyasachi, "A Three-Phase Hybrid Cascaded Modular Multilevel Inverter for Renewable Energy Environment," *IEEE Trans. Power. Electron.*, vol. 32, no. 2, pp. 1070–1087, Feb. 2017.

[4] S. S. Fazel, S. Bernet, D. Krug and K. Jalili, "Design and comparison of 4-kv neutral-point-clamped, flflying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, Jul./Aug. 2007.

[5] S. R. Pulikanti and V. G. Agelidis, "Control of neutral point and flying capacitor voltages in five-level SHE-PWM controlled ANPC converter," *in Proc.4th ICIEA*, May 25-27, 2009, pp. 172-177.

[6] F. Z. Peng, J. S. Lai, J. McKeever and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static var generation," *in Proc. IEEE/IAS Annu. Meeting, Orlando, FL*, Oct. 8-12, 1995, pp. 2541-2548.

[7] Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.

[8] Y. Ye, K. W. E. Cheng, J. Liu and K. Ding, "A Step-Up Switched Capacitor Multilevel Inverter With Self-Voltage Balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014.

[9] E. Babaei, and S. S. Gowgani, "Hybrid Multilevel Inverter Using Switched Capacitor Units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014.

[10] R. Barzegarkhoo, H. M. Kojabadi1, E. Zamiry, N. Vosooghi and L. Chang, "Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5604-5617, Aug. 2016.

[11] T. Roy, P. K. Sadhu and A. Dasgupta, "Cross-Switched Multilevel Inverter Using Novel Switched Capacitor Converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8521-8532, Nov. 2019.

[12] A. Taghvaie, J. Adabi and M. Rezanejad, "A Self-Balanced Step-Up Multilevel Inverter Based on Switched-Capacitor Structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.

[13] M. Saeedian, M. E. Adabi, S. M. Hosseini, J. Adabi and E. Pouresmaeil, "A Novel Step-Up Single Source Multilevel Inverter: Topology, Operating Principle, and Modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3269–3282, April 2019.

[14] Y. Ye, W. Peng and Y. Yi, "Analysis and Optimal Design of Switched-Capacitor Seven-Level Inverter With Hybrid PWM Algorithm," *IEEE Trans. Ind. Informat.*, vol. 16, no. 8, pp. 5276-5285, Aug. 2020.

[15] Y. Ye, S. Chen, X. Wang and K. W. E. E. Cheng, "Self-Balanced 13-Level Inverter Based on Switched-Capacitor Structure and Hybrid PWM Algorithm," *IEEE Trans. Ind. Electron.* doi: 10.1109/TIE.2020.2989716.

[16] K. Kim, J. Han and G. Moon, "A High Step-Up Switched-Capacitor 13-Level Inverter with Reduced Number of Switches," *IEEE Trans. Power Electron.* doi: 10.1109/TPEL.2020.3012282.

[17] N. Sandeep, "A 13-Level Switched-Capacitor-Based Boosting Inverter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, doi: 10.1109/TCSII.2020.3017338.

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